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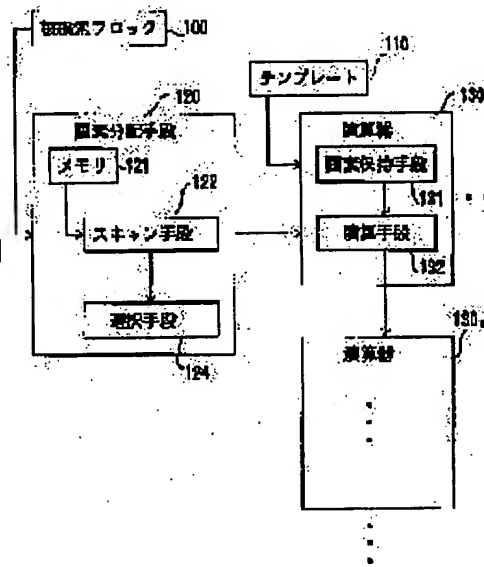
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## (54) MOVEMENT COMPENSATED ARITHMETIC UNIT

### (57)Abstract:

PURPOSE: To provide a movement compensated arithmetic unit which can efficiently transfer picture elements without generating any disturbance in a pipe line while simple constituting a computing element.

CONSTITUTION: This unit is provided with a pixel selection means 120 equipped with a first scanning means 122, a second scan means and selective means 124 for selecting any picture element inside a block 100 to be searched and sending the picture element, and  $m \times n$  pieces of computing elements 130 equipped with a pixel holding means 131 for holding the picture element in a template 110 allocated to every computing element 130, and an arithmetic means 132 for calculating a differential absolute value or a differential square value between the pixel of the pixel holding means and the pixel selected by the pixel distributing means, afterwards, to add that value and the intermediate value of L1 norm or L2 norm sent from the preceding computing element and for transferring the added value to the next computing element.



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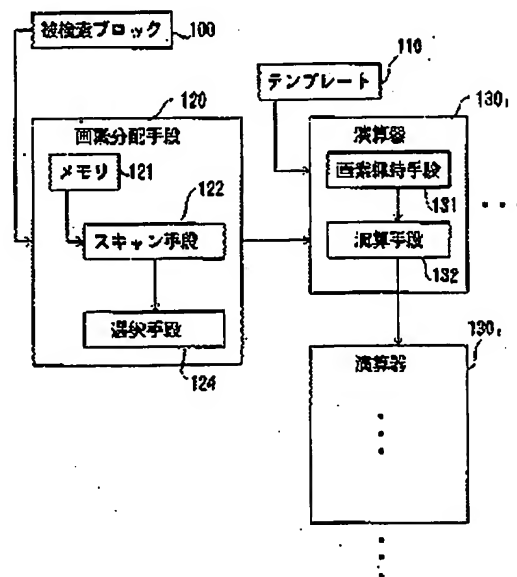
(54)【発明の名称】 動き補償演算装置

(57)【要約】

【目的】 本発明の目的は、簡易な演算器の構成とし、かつパイプラインに乱れが生じることなく、効率よく画素転送することができる動き補償演算回路を提供することである。

【構成】 本発明は、第1のスキャン手段122と第2のスキャン手段123と被探索ブロック100内の画素を選択して送出する選択手段124とを有する画素選択手段120と、演算器130毎に割り当てられたテンプレート110内の画素を保持する画素保持手段131と画素保持手段131の画素と画素選択手段131によって選択された画素との差分絶対値または、差分自乗値を計算した後、前の演算器から送られてくる1ノルムまたは2ノルムの中間値とを加算し、加算値を次の演算器に転送する演算手段132を含む $m \times n$ 個の演算器130とを有する。

本発明の原理構成図



## 【特許請求の範囲】

【請求項1】 現フレーム中の $m$ 画素 $\times n$ ラインの画素ブロックであるテンプレートと、探索領域内の水平または、垂直方向に1画素づつずれた $m$ 画素 $\times n$ ラインの全ての画素ブロック（被探索画素ブロック群）との間で、画素ブロック内の対応する画素の差分絶対値和である $L1$ ノルムまたは、差分自乗和である $L2$ ノルムを計算する演算器を含む動き補償演算装置において、前フレーム中の画素を保持するメモリと、該メモリから前フレーム中の $(a-m-1)$ 画素 $\times b$ ラインの探索領域を $m$ 画素 $\times b$ ラインの領域に分割して得られる $a$ 個の領域（右端の領域は $m-1$ 画素 $\times b$ ライン）のうち、左端の領域の一番上のラインの左端の画素から1画素づつ読み出し、 $m$ 画素読み出すと、隣の領域から1画素づつ読み出すことを開始し、 $m-1$ 画素読み出すまで続けると同時に、左端の領域内でも1ライン下に移り左端の画素から1画素づつ読み出すことを開始し、 $m$ 画素読み出す、即ち、同時に2画素読み出すことを左端の領域内の $m \times b$ 画素とその隣の領域内の $(m-1) \times b$ 画素を読み出し終えるまで続け、第1回目のスキャン終了後、第1回目のスキャンにおいて、 $(m-1) \times b$ 画素を読み出した領域の一番上のラインの左端の画素を開始点として同様の2回目のスキャンを行い、探索領域内全体をスキャンするまで計 $a-1$ 回のスキャンを繰り返すスキャン手段と、該スキャン手段が行われる間に該メモリから読み出される2画素のうち、個々の該演算器に割り当てられたテンプレート内の画素に対応する被探索ブロック内の画素を選択して該演算器に送出する選択手段とを有する画素分配手段と、該演算器毎に割り当てられた該テンプレート内の画素を保持する画素保持手段と、該画素保持手段に保持している該テンプレート内の画素と、該画素分配手段によって分配された画素との差分絶対値または、差分自乗値を計算した後、前の演算器から送られてくる $L1$ ノルムまたは $L2$ ノルムの中間値とを加算し、加算値を次の演算器に転送する演算手段とを含む $m \times n$ 個の演算器とを有す\*

$$L1 \text{ ノルム} = \sum |X_j(i) - Y(i)| \quad i = 0-15 \quad (1)$$

$$L2 \text{ ノルム} = \sum (X_j(i) - Y(i))^2 \quad i = 0-15 \quad (2)$$

ここで、 $j$ は複数の被探索ブロックにつけられた番号を表し、 $X_j(i)$ は、前フレーム2から切り出した被探索ブロック $j$ 中の画素である。図13中では、被探索ブロックとして画素ブロック3~6を示す。 $j=4\sim7$ の画素ブロックは水平方向に1画素ずれているのみであり、大部分の画素は共通である。また、 $Y(i)$ はテンプレート1中の画素である。

【0006】次に、上記(1)式 または(2)式によって計算された $L1$ ノルムまたは、 $L2$ ノルムが最小となる被探索ブロックの番号 $j$ とその最小値を求める。以上が動き補償で行われる演算である。

【0007】上記の動き補償に関する技術については、

＊ることを特徴とする動き補償演算装置。

【請求項2】 前記画素分配手段を含み、上下左右に隣接したテンプレート内の画素を交互に選択して前記画素分配手段により分配された画素との間で差分絶対値または、差分自乗値を計算し、該上下左右に隣接したテンプレートと被探索ブロック間の $L1$ ノルムまたは $L2$ ノルムを得る時間的多重手段を有する動き補償演算装置において、

被探索ブロック内の画素を多重化した回数だけ差分絶対値または、差分自乗値の計算に使用している間に、前記画素分配手段により次の計算に使用する被探索ブロックの内の画素を分配して個々の演算器内の予備のレジスタに送る第1のレジスタ転送手段と、

差分絶対値または差分自乗値の計算に使用するタイミングで実際に差分絶対値または、差分自乗値の計算に使用するレジスタに移す第2のレジスタ転送手段とを有することを特徴とする動き補償演算回路。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明は、動き補償演算回路に係り、特に、動画像符号化処理中の動き補償を全探索法で行う動き補償演算装置に関する。

## 【0002】

【従来の技術】従来の動き補償演算回路において、4画素 $\times 4$ ラインの画素ブロックを例として説明する。

## 【0003】(1) 動き補償

動き補償の対象となる画素ブロックについて説明する。図13は動き補償演算の対象となる被探索画素ブロックとテンプレートを示す図である。

【0004】まず、テンプレート1と前フレーム2中の決められた探索領域の中の被探索ブロック間で以下に示す式により画素ブロック内の対応する画素の差分絶対値和である $L1$ ノルムまたは、差分自乗和である $L2$ ノルムのいずれかを計算する。

## 【0005】

例えば、M.Yamashina, T. Enomoto, T. Kunio, I. Tmaitani, H. Harasaka, Y. Endo, T. Nishitani, M. Sato, K. Kikuchi, "A Microprogrammable, Real-Time Video Signal Processor (VSP) for Motion Compensation", IEEE J. Solid-State Circuits, vol. SC-23, pp. 907-915, Aug. 1988. に記載されている。

【0008】上記の $L1$ ノルムと $L2$ ノルムの違いは、2画素の差を計算した後、絶対値をとるか乗算するかだけであるので、以下では $L1$ ノルムを用いた場合についてのみ説明する。

【0009】(2) 被探索ブロック間の画素の重なり全探索法においては、探索領域中から水平または垂直方

向に1画素づつずれた画素ブロックを切り出し、被探索ブロック群とする。従って、被探索ブロック間の画素には重なりがある。

【0010】図14は被探索画素ブロック間の重なりを示す図である。

【0011】前フレーム7は16画素×16ラインから成り、テンプレート8から±3画素の範囲を探索する。この場合、探索領域9は10画素×10ラインとなり、探索領域9内における被探索ブロックの総数は49である。図14に示された被探索ブロック10~13は水平方向に1画素づつずれており、画素 $X_{1,1}$ 、 $X_{1,2}$ 、 $X_{1,3}$ 、 $X_{1,4}$ はこれら4ブロックに共通に含まれている。また、被探索ブロック10、14~16は垂直方向に1ラインづつずれており、画素 $X_{1,1}$ 、 $X_{2,1}$ 、 $X_{3,1}$ 、 $X_{4,1}$ はこれら4ブロックに共通に含まれている。特に、画素 $X_{1,1}$ は計16個の被探索ブロックに共通に含まれている。従って、前フレーム8の画素が書き込まれているメモリから1画素読み出すと、その画素は最大4×4回のL1ノルムの計算に利用できる。

【0012】(3) 探索領域間の画素の重なり  
図15は隣接したテンプレートに対する探索領域の重なりを示す。 $X_{1,1}$ 、 $X_{1,2}$ 、 $X_{1,3}$ 、 $X_{1,4}$ で囲まれた画素群は、テンプレート17に対する探索領域20とテンプレート8に対する探索領域9に共通に含まれている。さらに、 $X_{2,1}$ 、 $X_{2,2}$ 、 $X_{2,3}$ 、 $X_{2,4}$ で囲まれた画素群は探索領域20、9、21、22に共通に含まれている。従って、上記の被探索ブロック間の画素の重なりから得られる4×4回と合わせると、前フレーム7の画素が書き込まれているメモリから1画素読み出すと、その画素は最大4×4×4回のL1ノルムの計算に利用できる。

【0013】以下に従来の技術の例について説明する。

【0014】(4) 従来の技術-1

図16は動き補償を全探索法で計算する従来技術の第1の例の装置を説明するための図を示す。

【0015】同図において、前フレーム中の画素は2出力ポート(P0、P1)を持ったメモリ23に置かれている。図16中に示す水平方向に1画素づつずれた被探索ブロック24~27のL1ノルムを計算する場合を考える。テンプレート中の画素は1出力ポート(P2)を持ったメモリ30に置かれている。PE28はL1ノルムを計算する演算回路である。セレクタ29は、メモリ23の出力ポートP0とP1から同図に示す順番で読み出された画素から被探索ブロック24~27内の画素を選択し、それぞれPE0~PE3に送る。

【0016】図17は従来技術の第1の例のPE28の構成を示す。PE0の入力B<sub>1,1</sub>はメモリ30のP2に接続されている。メモリ30から読み出されたテンプレート中の画素はPE0のレジスタ33にラッチされた後、次々とPE間をシフトして転送される。このようにすると、各PE内ではテンプレート内の画素と被探索ブロッ

ク内の画素を読み込む順番が一致し、L1ノルムを計算することができる。

【0017】PE0が被探索ブロック24、PE1が被探索ブロック25、PE2が被探索ブロック26、PE3が被探索ブロック27を計算する場合の例について説明する。

【0018】図18は従来の技術の第1の例における画素の流れを示す。同図中、点線で囲まれた画素は出力ポートP1、それ以外は出力ポートP0から読み出された画素である。また、同図中にはL1ノルム計算の対象となる被探索ブロックを $X_1(0,0)$ となる画素の番号で代表させ、各PE28がそのL1ノルムを計算中であることをL20、L21等として示している。計算されたL1ノルムは出力Cより最小値検出器31に送られる。

【0019】即ち、図16に示した装置は、水平方向に1画素づつずれた被探索ブロック間の画素の1次元の重なりを利用してメモリ23から読み出した画素をPE28に放送し、4並列でL1ノルムを計算する。

【0020】上記の従来装置の第1の例に関する技術については、例えば、K.M. Yang, M.T. Sun, L.Wu, "Family of VLSI Designs for the motion Compensation Block-Matching Algorithm", IEEE Trans. Circuits and Systems, vol. CAS-36, No.10, pp1317-1325, Oct. 1989に記載されている。

【0021】(5) 従来の技術-2

動き補償を全探索法で計算する従来技術の第2の例を説明する。

【0022】図19は動き補償を全探索法で計算する従来技術の第2の例の装置を説明するための図を示す。同図の装置は、4×4=16個のPE28を持っている点を除き、上記の従来技術の第1の例と同一の構成である。PE0~PE3が従来の技術の第1の例同様、被探索ブロック24~27を計算し、さらに、PE4が被探索ブロック32、PE8が被探索ブロック33、PE12が被探索ブロック34を計算する場合を考え、その場合の被探索ブロック内とテンプレート内の画素の流れを説明する。

【0023】図20は、従来の技術の第2の例における画素の流れを示す。

【0024】本構成では、PE0、PE1、PE2、...、PE15において順次L20、L21、L22、...、L71の計算が終了したら連続してPE0、PE1、...、PE11において、L84、L85、...、L119の計算を開始することができる。そこで、メモリ30から読み出され、PE間をシフトしているテンプレート17内の画素をPE15からPE0にフィードバックするパスを設け、テンプレート17内の画素を再度読み出すことを不要としている。但し、図15に示した探索領域20内の全L1ノルムを計算するため

には、図20に示すL20の計算で始まり、L119の計算で終わる被探索ブロック群のスキャン（以下右スキャンと記す）だけでなく、その左側のL16の計算で始まり、L115の計算で終わる被探索ブロック群のスキャン（以下左スキャンと記す）が必要である。しかし、L115の計算はPE11で行われるため、左スキャンから右スキャンに移るとき、図20に示したように、テンプレート17内の画素のPE15からP0へのフィードバックが途切れる。そのためテンプレート17ないの画素のメモリ30から再読み出しが必要となる。

【0025】すなわち、図19に示した装置は、水平に1画素づつ垂直方向に1ラインづつずれた被探索ブロック間の画素の2次元の重なりを利用してメモリ28から読み出した画素をPEに放送し、 $4 \times 4$ 並列でL1ノルムを計算する。

【0026】上記従来装置の第2の例に関する技術については、例えば田代、南、笠井、金子“高並列動き補償演算器”（特願平4122274）に記載されている。

【0027】(6) 従来技術-3

動き補償を全探索法で計算する従来技術の第3の例を説明する。

【0028】図21は、動き補償を全探索法で計算する従来技術の第3の例の装置を説明するための図を示す。

【0029】同図に示した装置は、上記の従来技術の第2の例の装置において、テンプレートを保持していたメモリ30を2出力ポート（P3、P4）を持ったメモリ39に置き換え、さらに $4 \times 4$ 個のPE28と1個の最小値検出器31を追加した構成である。

【0030】図22は従来技術の第3の例における画素の流れを示す。上記の(3)の探索領域間の画素の重なりで示したように、隣接したテンプレートに対する探索領域には重なりがある。従って、図22に示すように同一の被探索ブロックに対して2個のL1ノルムを並列に計算することができる。

【0031】即ち、図21に示した装置は、被探索ブロック群のメモリ23からの読み出しは従来技術の第2の例と同一でありながら、 $4 \times 4 \times 2$ 並列でL1ノルムを計算することができる。

【0032】上記の従来技術の第3の例に関する技術については、上記従来技術の第1の例と同じく、例えば、K.M.Yang, M.T.Yang, M.T.Sun, L.Wu, "A Family of VLSI Designs for the Motion Compensation Block-Matching Algorithm", IEEE Trans. Circuits and Systems, vol.CAS-36, no. 10, pp1317-1325, Oct, 1989, に記載されている。

【0033】

【発明が解決しようとする課題】しかしながら、上記従来技術の第1～第3の例で用いたPE28は内部に累算器を持ったため、構造が複雑であり新たなL1ノルムの計算を開始する前に、累算値を保持しているレジスタ3

7の初期化が必要であるという問題がある。また、個々のPE28内でL1ノルムを計算した後、最小値検出器31にL1ノルムを転送する構成であるため、全PE28から最小値検出器31へのバスが必要であるという問題がある。

【0034】さらに、従来技術の第1～第3の例において説明したように、被探索ブロック数が $4 \times 4$ の整数倍でない場合には、シフトが完全になされていないためPE28間をシフトしているテンプレート内の画素のフィードバックに乱れが生じるという問題がある。

【0035】以上は、PEの構造から発生する問題であるが、さらに、被探索ブロックの1回のスキャン当り2画素を前フレームの画素を保持するメモリから読み出し、L1ノルム計算用の全ての演算器に放送するという画素の分配から発生する問題がある。即ち前フレームの画素を保持するメモリ23に2個の出力ポートが必要であり、また、探索領域の画素を前PE28に放送するバスは最後のPE28がL1ノルムの計算を終了するまで空かないため、PE0の計算終了後、再度計算を開始するまで無効サイクルが生じるという問題がある。

【0036】本発明は、上記の点に鑑みなされたもので、全PEから最小値検出器へのバスが不要で、さらに、テンプレート内の画素のフィードバックバスが不要で、また、PE0の計算終了後、計算を再開するまでの無効サイクルが生じず、L1ノルムを計算する演算器の構造が簡素化され、さらに、メモリの出力ポートが1つで済むような動き補償を全探索法で行う動き補償演算装置を提供することを目的とする。

【0037】

【課題を解決するための手段】図1は本発明の原理構成図を示す。

【0038】本発明は、現フレーム中の $m$ 画素 $\times n$ ラインの画素ブロックであるテンプレート110と、探索領域内の水平または、垂直方向に1画素づつずれた $m$ 画素 $\times n$ ラインの全ての画素ブロック（被探索画素ブロック群）100との間で、画素ブロック内の対応する画素の差分絶対値和であるL1ノルムまたは、差分自乗和であるL2ノルムを計算する演算器を含む動き補償演算装置において、前フレーム中の画素を保持するメモリ121と、メモリ121から前フレーム中の $(a, m-1)$ 画素 $\times b$ ラインの探索領域を $m$ 画素 $\times b$ ラインの領域に分割して得られる $a$ 個の領域（右端の領域は $m-1$ 画素 $\times b$ ライン）のうち、左端の領域の一番上のラインの左端の画素から1画素づつ読み出し、 $m$ 画素読み出すと、隣の領域から1画素づつ読み出すことを開始し、 $m-1$ 画素読み出すまで続けると同時に、左端の領域内でも1ライン下に移り左端の画素から1画素づつ読み出すことを開始し、 $m$ 画素読み出す、即ち、同時に2画素読み出すことを左端の領域内の $m \times b$ 画素とその隣の領域内の $(m-1) \times b$ 画素を読み出し終えるまで続ける第1回目の

スキャン終了後、第1回目のスキャンにおいて、 $(m-1) \times n$ 画素を読み出した領域の一番上のラインの左端の画素を開始点として同様の第2回目のスキャンを行い、探索領域内全体をスキャンするまで計 $a-1$ 回のスキャンを繰り返すスキャン手段122と、スキャン手段122が行われる間にメモリ121から読み出される2画素のうち、個々の演算器130に割り当てられたテンプレート110内の画素に対応する被探索ブロックの画素を選択して演算器130に送出する選択手段124とを有する画素分配手段120と、演算器130毎に割り当てられたテンプレート110内の画素を保持する画素保持手段131と、画素保持手段131に保持しているテンプレート110内の画素と、画素分配手段120によって分配された画素との差分絶対値または、差分自乗値を計算した後、前の演算器から送られてくるL1ノルムまたはL2ノルムの中間値とを加算し、加算値を次の演算器に転送する演算手段132とを含む $m \times n$ 個の演算器130とを有する。

【0039】また、本発明は、画素分配手段を含み、上下左右に隣接したテンプレート内の画素を交互に選択して前記画素分配手段により分配された画素との間で差分絶対値または、差分自乗値を計算し、該上下左右に隣接したテンプレートと被探索ブロック間のL1ノルムまたはL2ノルムを得る時間的多重手段を有する動き補償演算装置において、被探索ブロック内の画素を多重化した回数だけ差分絶対値または、差分自乗値の計算に使用している間に、前記画素選択手段により次の計算に使用する被探索ブロックの内の画素を選択して個々の演算器内の予備のレジスタに送る第1のレジスタ転送手段と、差分絶対値または差分自乗値の計算に使用するタイミングで実際に差分絶対値または、差分自乗値の計算に使用するレジスタに移す第2のレジスタ転送手段とを有する。

【0040】

【作用】本発明は、全PEから最小値検出器へのバスが不要で、さらに、テンプレート内の画素のフィードバックバスが不要で、また、PE0の計算終了後、計算を再開するまでの無効サイクルが生じず、L1ノルムを計算する演算器の構造が簡素化され、さらに、メモリの出力ポートが1つで済む。

【0041】

【実施例】

（第1の実施例）図2は本発明の第1の実施例の演算器の構成を示す。図3は本発明の第1の実施例の装置を説明するための図を示す。図2において、演算器SA41はレジスタ41、43、35、45と差分絶対値演算器34、加算器44より構成され、Aより入力された画素がレジスタ42に入力され、Bより入力された画素がレジスタ43に入力され、差分絶対値演算器34によりレジスタ42とレジスタ43の差分絶対値を計算し、レジスタ35に出力する。次に、レジスタ35の差分絶対値

と、Cより入力された値を加算器44で加算し、その加算値をレジスタ45に入力する。その値は、レジスタ45から出力ポートDを介して次の演算器にまたは、最小値検出器31に出力される。

【0042】従来技術の第1～第3の例で用いたPE28ではテンプレート内の画素がPE間をシフトしたのに対し、本構成では、演算の中間値がSA41間をシフトする。図4は被探索ブロック内とテンプレート内の画素の流れを示す。被探索ブロック内の画素の流れは従来技術の第1～第3の例と同一である。一方テンプレート内の画素については、メモリ30からの読み出しは従来技術の第1～第3の例と同一であるが、 $Y_{0,0} = (Y(0))$ はSA0内のレジスタ43、 $Y_{0,1} = (Y(1))$ はSA1内のレジスタ43、…… $Y_{1,15} = Y(15)$ はSA15内のレジスタ43にラッチされ、そのまま保持される。

【0043】説明の都合上、図4には被探索ブロック群を右スキャンする場合だけを示してある。実際には、左スキャンにつづいて右スキャンが行われるが、本構成にはPE15からPE0にフィードバックするバスがないため、従来技術の第2、第3の例で問題となった左スキャンから右スキャンに移るときのパイプラインの乱れが生じない。そのため、左スキャンから右スキャンに移るときにもテンプレート17内の画素のメモリ30からの再読み出しは不要である。

【0044】（第2の実施例）図5は本発明の第2の実施例の演算器を示す。図6は本発明の第2の実施例の演算装置を説明するための図を示す。

【0045】本実施例は、従来技術の第3の例同様に、隣接したテンプレートに対する探索領域には重なりがあることを利用して、同一の被探索ブロックに対して2個のL1ノルムを計算する。但し、従来技術の第3の例では並列計算するために2倍の数のPEを用いたが、本実施例では、時間的に多重化して計算する。

【0046】即ち、DSA46内でテンプレート内の画素を保持するレジスタ51、52、L1ノルムの中間値をシフトするレジスタ53、54をそれぞれ2個設け、隣接した2個のテンプレートに対するL1ノルムを交互に計算する。

【0047】図7は本発明の第2の実施例の画素の流れを示す。この構成では、被探索ブロック内の画素を2回L1ノルムの計算に使うことになるため、画素の転送に1サイクル毎に空きが生じる。従来技術の第1～第3の例では、被探索ブロックの画素を全PE28に分配するバスが最後のPE28のL1ノルム計算終了まで空かないため、PE0の計算終了後、再度計算を開始するまで無効サイクルが生じるという問題があったが、本実施例の構成では、この空きサイクルを利用して次の被探索領域のスキャンによる画素を転送することができる。

【0048】DSA46内のレジスタ47において空き

サイクルに転送される画素をラッチし、L1ノルムの計算をその画素で行うタイミングでレジスタ48に転送する。レジスタ48にラッチされた画素とレジスタ51と52に保持されている異なるテンプレート内の画素を用いてL1ノルムを計算する。そして計算されたL1ノルムは、2個のテンプレートに対応して設けられた最小値検出器31に送られる。なお、図7中における水平方向の矢印はレジスタ47にラッチした画素をレジスタ48に転送することを意味する。また、右斜め下方向の矢印はL1ノルムの中間値が転送されて行くことを意味する。

【0049】(第3の実施例) 図8は本発明の第3の実施例の演算器の構成を示す。図9は本発明の第3の実施例の演算装置を説明するための図を示す。

【0050】本実施例では、上下左右に隣接したテンプレートに対する探索領域には重なりがあることを利用して、同一の被探索ブロックに対して4個のL1ノルムを時間的に多重化して計算する。即ち、FSA55内で4個の異なるテンプレート内の画素を保持するレジスタ56、57、58、59、L1ノルムの中間値をシフトするそれぞれ4個のレジスタ60、61、62、63を設け、上下左右に隣接した4個のテンプレートに対するL1ノルムを交互に計算する。

【0051】図10は本発明の第3の実施例の画素の流れを示す。この構成は、被探索ブロック内の画素を4回L1ノルムの計算に使用することになるため、1画素の転送につき、3サイクルの空きが生じる。従って、本実施例では、上記の第2の実施例と同様に、この空きサイクルを利用して次の被探索領域のスキャンによる画素を転送することができることに加えて、上記の第2の実施例では並列に転送していた被探索領域のスキャンによる2個の画素を時間をずらして転送することにより、画素を選択するためのセクタ29が不要となり、さらに、前フレーム中の画素を保持するメモリ65も1つの出力ポート(P5)を持つだけでよくなる。

【0052】なお、図7同様、図10中における水平方向の矢印はレジスタ47にラッチした画素をレジスタ48に転送することを意味する。また、右斜め下方向の矢印はL1ノルムの中間値が転送されて行くことを意味する。

【0053】(第4の実施例) 図11は本発明の第4の実施例の演算器FPE66の構成を示す。図12は本発明の第4の実施例の演算装置を説明するための図を示す。

【0054】図11に示す演算器FPE66は探索領域をスキャンし、メモリ65から読み出した画素の分配及びレジスタ47と48の間の転送については、上記の第3の実施例と同一である。一方テンプレート内の画素は、入力B<sub>11</sub>からレジスタ67に入力され、レジスタ68、69、70をシフトした後、次の演算器FPE66

に転送される。ここで、差分絶対値演算器34はセクタ49が選択した信号とレジスタ67の信号の差分絶対値を算出し、レジスタ35に転送する。レジスタ71、72、73、74は、上下左右に隣接した4個のテンプレートに対するL1ノルムの中間値が保持されており、加算器44は4個のテンプレートに対するL1ノルムを交互に計算する。

【0055】本実施例は、上記の第3の実施例同様、同一の被探索ブロックに対して4個のL1ノルムを時間的に多重化して計算するが、従来技術の第1～第3の例で用いたPE同様、テンプレート内の画素がFPE66間をシフトし、個々のFPE66内でL1ノルムの中間値を累算する構造である。

【0056】なお、上記の実施例では、簡単のために4画素×4ラインのテンプレートに対して4×4並列演算を行う場合についてのみ説明したが、本発明はm画素×nラインのテンプレートに対して、m×n並列演算を行う場合に対しても適用できる。

【0057】

【発明の効果】 上述のように、本発明によれば、L1ノルム計算用の個々の演算器内に累算用のフィードバックが不要となる。また、最小値検出器へのバスは最終的にm×n個の差分絶対値が得られる演算器にのみ設ければよく、L1ノルムを計算する演算器の構造が単純になるという効果がある。さらに、被探索ブロック内の画素を1回スキャンする時に計算する被探索ブロック数がm×nの整数倍でない場合にも、L1ノルム計算用演算器間のパイプラインに乱れが生じないという効果がある。

【0058】さらに、上下左右に隣接したテンプレートに対するL1ノルムを時間的に多重化して計算することにより、被探索領域内の画素を転送するバスに空きサイクルが生じる。この空きサイクルを利用して次の被探索領域のスキャンによる画素を転送することができ、最初の演算器が1回のスキャンに対するL1ノルムの計算を終了すると、最後の演算器がそのスキャンに対するL1ノルムの計算を終了することを待つことなく、次のスキャンに対するL1ノルムの計算を始めることができるという効果がある。

【0059】さらに、1つのスキャンにおける被探索ブロック内の2個の画素を時間をずらして転送することにより、画素を分配するバスが単純になり、前フレーム中の画素を保持するメモリも1出力ポートを持つだけでよい。

【図面の簡単な説明】

【図1】 本発明の原理構成図である。

【図2】 本発明の第1の実施例の演算器の構成図である。

【図3】 本発明の第1の実施例の演算装置を説明するための図である。

【図4】 本発明の第1の実施例の画素の流れを示す図で



ある。

【図5】本発明の第2の実施例の演算器の構成図である。

【図6】本発明の第2の実施例の演算装置を説明するための図である。

【図7】本発明の第2の実施例の画素の流れを示す図である。

【図8】本発明の第3の実施例の演算器の構成図である。

【図9】本発明の第3の実施例の演算装置を説明するための図である。

【図10】本発明の第3の実施例の画素の流れを示す図である。

【図11】本発明の第4の実施例の演算器の構成図である。

【図12】本発明の第4の実施例の演算装置を説明するための図である。

【図13】動き補償演算の対象となる被探索画素のブロックとテンプレートを示す図である。

【図14】被探索画素ブロック間の重なりを示す図である。

【図15】隣接したテンプレートに対する探索領域の重なりを示す図である。

【図16】従来技術の第1の例の装置を説明するための図である。

【図17】従来技術の第1～第3の例で用いられた演算器の構成図である。

【図18】従来技術の第1の例における画素の流れを示す図である。

【図19】従来技術の第2の例の装置を説明するための図である。

【図20】従来技術の第2の例における画素の流れを示す図である。

【図21】従来技術の第3の例の装置を説明するための図である。

【図22】従来技術の第3の例における画素の流れを示す図である。

【符号の説明】

1, 8, 17, 18, 19, 40, 64 テンプレート

2, 7 前フレーム

3, 4, 5, 6, 10, 11, 12, 13, 14, 1

5, 16, 24, 25, 26, 27, 32, 33, 34

被探索画素ブロック

9, 20, 21, 22 探索領域

23 前フレーム中の画素を保持する2出力ポートを持ったメモリ

28 従来技術の第1～第3の例で用いられた演算器

29, 35, 49, 50 セレクタ

30 テンプレートを保持する1出力ポートをもったメモリ

31 最小値検出器

32, 33, 35, 27, 42, 43, 45, 47, 4

8, 51, 52, 53

54, 56, 57, 58, 59, 60, 61, 62, 6

3, 67, 68, 69

70, 71, 72, 73, 74 レジスタ

34 差分絶対値演算器

36, 44 加算器

38 ライスチートバッファ

39 テンプレートを保持する2出力ポートを持ったメモリ

41 本発明の第1の実施例で用いる演算器

46 本発明の第2の実施例で用いる演算器

55 本発明の第3の実施例で用いる演算器

65 前フレーム中の画素を保持する1出力ポートを持ったメモリ

66 本発明の第4の実施例で用いる演算器

100 被探索ブロック

110 テンプレート

120 画素選択手段

121 メモリ

122 第1のスキャン手段

123 第2のスキャン手段

124 選択手段

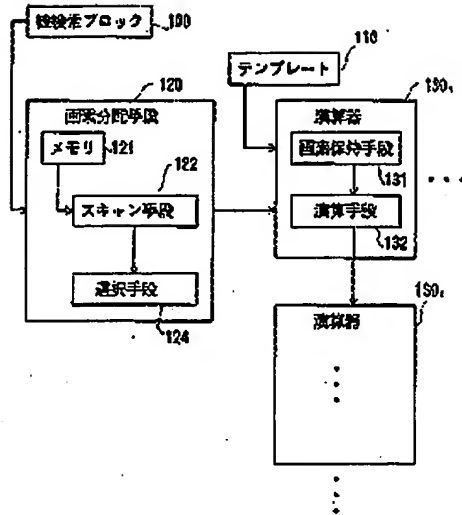
130 演算器

131 画素保持手段

132 演算手段

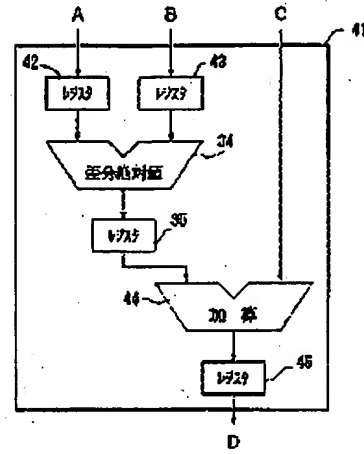
【図1】

本発明の原理構成図



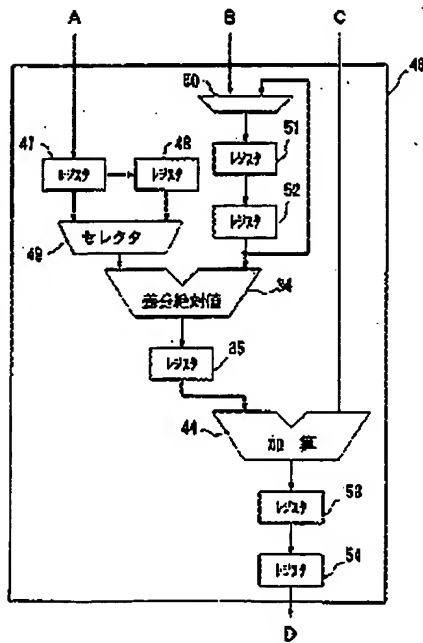
【図2】

本発明の第1の実施例の演算器の構成図



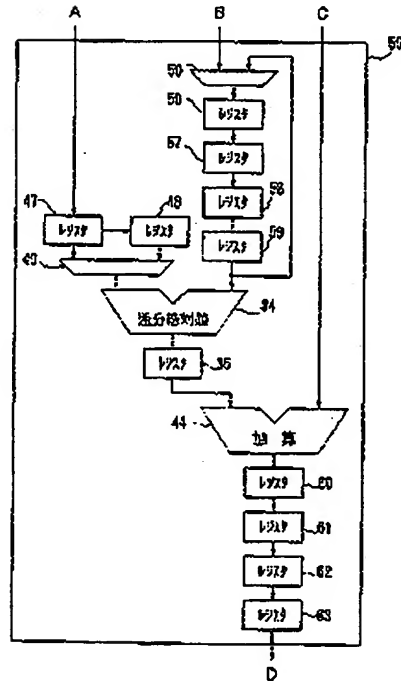
【図5】

本発明の第2の実施例の演算器を示す図



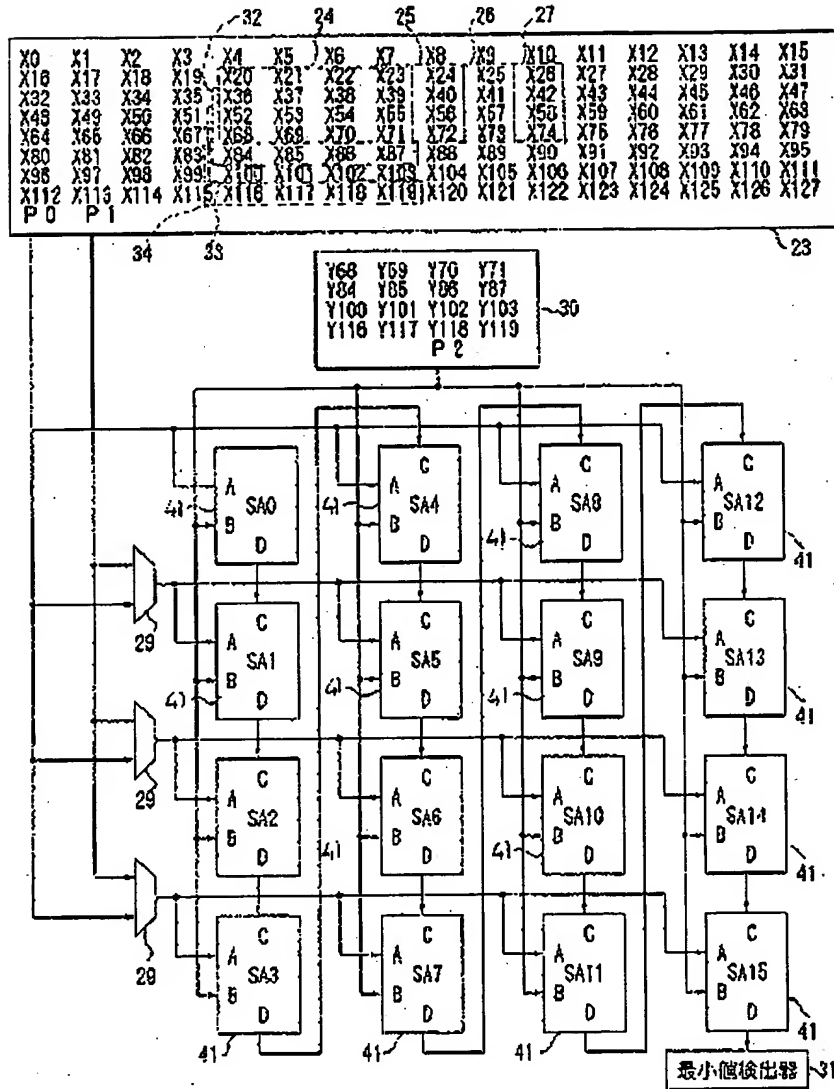
【図8】

本発明の第2の実施例の演算器の構成図



【図3】

本発明の第1の実施例の装置を説明するための図

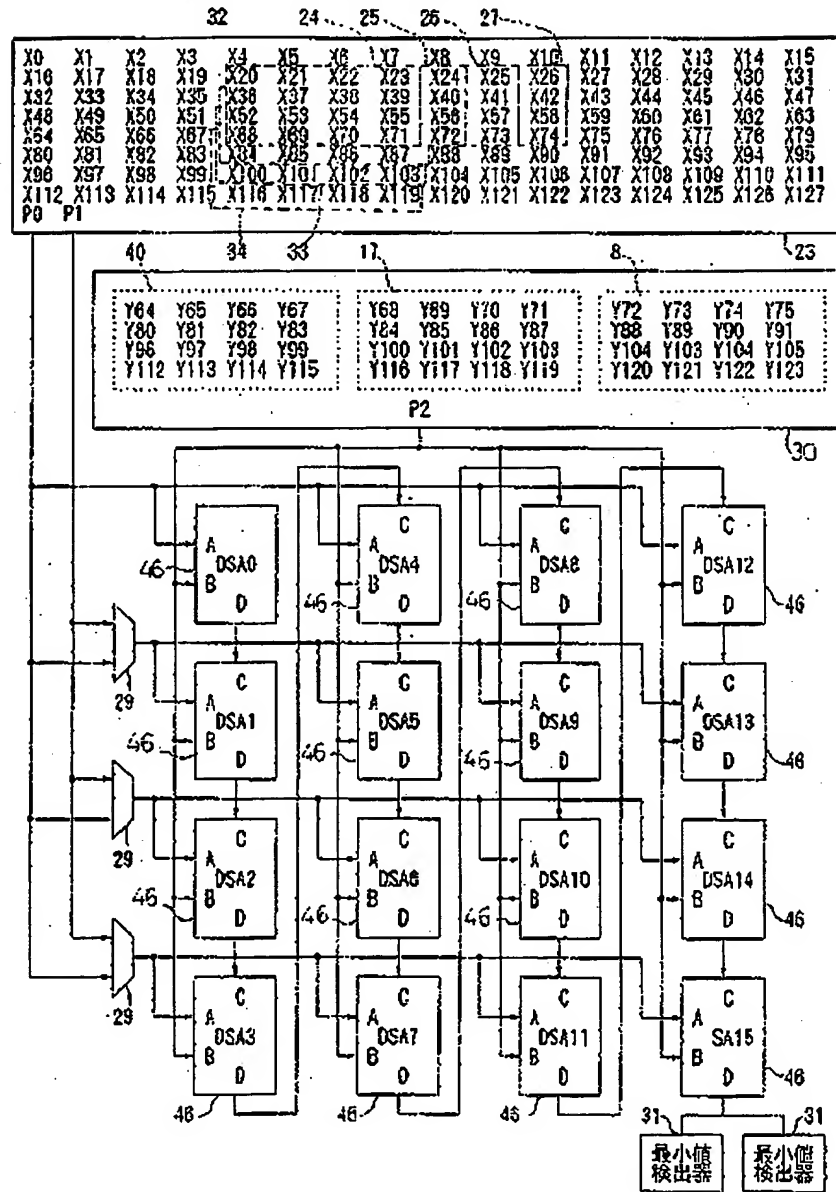


本発明の第１の実施例の画素の流れを示す図

P0 P1 P2	X20 Y68	X21 Y69	X22 Y70	X23 Y71	X24 Y72	X25 Y73	X26 Y74	X27 Y75	X28 Y76	X29 Y77	X30 Y78	X31 Y79	X32 Y80	X33 Y81	X34 Y82	X35 Y83	X36 Y84	X37 Y85	X38 Y86	X39 Y87	X40 Y88	X41 Y89	X42 Y90	X43 Y91	X44 Y92	X45 Y93	X46 Y94	X47 Y95	X48 Y96	X49 Y97	X50 Y98	X51 Y99	X52 Y00	X53 Y01	X54 Y02	X55 Y03	X56 Y04	X57 Y05	X58 Y06	X59 Y07	X60 Y08	X61 Y09	X62 Y10	X63 Y11	X64 Y12	X65 Y13	X66 Y14	X67 Y15	X68 Y16	X69 Y17	X70 Y18	X71 Y19	X72 Y20	X73 Y21	X74 Y22	X75 Y23	X76 Y24	X77 Y25	X78 Y26	X79 Y27	X80 Y28	X81 Y29	X82 Y30	X83 Y31	X84 Y32	X85 Y33	X86 Y34	X87 Y35	X88 Y36	X89 Y37	X90 Y38	X91 Y39	X92 Y40	X93 Y41	X94 Y42	X95 Y43	X96 Y44	X97 Y45	X98 Y46	X99 Y47	Y00 Y48	Y01 Y49	Y02 Y50	Y03 Y51	Y04 Y52	Y05 Y53	Y06 Y54	Y07 Y55	Y08 Y56	Y09 Y57	Y10 Y58	Y11 Y59	Y12 Y60	Y13 Y61	Y14 Y62	Y15 Y63	Y16 Y64	Y17 Y65	Y18 Y66	Y19 Y67	Y20 Y68	Y21 Y69	Y22 Y70	Y23 Y71	Y24 Y72	Y25 Y73	Y26 Y74	Y27 Y75	Y28 Y76	Y29 Y77	Y30 Y78	Y31 Y79	Y32 Y80	Y33 Y81	Y34 Y82	Y35 Y83	Y36 Y84	Y37 Y85	Y38 Y86	Y39 Y87	Y40 Y88	Y41 Y89	Y42 Y90	Y43 Y91	Y44 Y92	Y45 Y93	Y46 Y94	Y47 Y95	Y48 Y96	Y49 Y97	Y50 Y98	Y51 Y99	Y52 Y00	Y53 Y01	Y54 Y02	Y55 Y03	Y56 Y04	Y57 Y05	Y58 Y06	Y59 Y07	Y60 Y08	Y61 Y09	Y62 Y10	Y63 Y11	Y64 Y12	Y65 Y13	Y66 Y14	Y67 Y15	Y68 Y16	Y69 Y17	Y70 Y18	Y71 Y19	Y72 Y20	Y73 Y21	Y74 Y22	Y75 Y23	Y76 Y24	Y77 Y25	Y78 Y26	Y79 Y27	Y80 Y28	Y81 Y29	Y82 Y30	Y83 Y31	Y84 Y32	Y85 Y33	Y86 Y34	Y87 Y35	Y88 Y36	Y89 Y37	Y90 Y38	Y91 Y39	Y92 Y40	Y93 Y41	Y94 Y42	Y95 Y43	Y96 Y44	Y97 Y45	Y98 Y46	Y99 Y47
S0	X20 Y68	X21 Y69	X22 Y70	X23 Y71	X24 Y72	X25 Y73	X26 Y74	X27 Y75	X28 Y76	X29 Y77	X30 Y78	X31 Y79	X32 Y80	X33 Y81	X34 Y82	X35 Y83	X36 Y84	X37 Y85	X38 Y86	X39 Y87	X40 Y88	X41 Y89	X42 Y90	X43 Y91	X44 Y92	X45 Y93	X46 Y94	X47 Y95	X48 Y96	X49 Y97	X50 Y98	X51 Y99	X52 Y00	X53 Y01	X54 Y02	X55 Y03	X56 Y04	X57 Y05	X58 Y06	X59 Y07	X60 Y08	X61 Y09	X62 Y10	X63 Y11	X64 Y12	X65 Y13	X66 Y14	X67 Y15	X68 Y16	X69 Y17	X70 Y18	X71 Y19	X72 Y20	X73 Y21	X74 Y22	X75 Y23	X76 Y24	X77 Y25	X78 Y26	X79 Y27	X80 Y28	X81 Y29	X82 Y30	X83 Y31	X84 Y32	X85 Y33	X86 Y34	X87 Y35	X88 Y36	X89 Y37	X90 Y38	X91 Y39	X92 Y40	X93 Y41	X94 Y42	X95 Y43	X96 Y44	X97 Y45	X98 Y46	X99 Y47	Y00 Y48	Y01 Y49	Y02 Y50	Y03 Y51	Y04 Y52	Y05 Y53	Y06 Y54	Y07 Y55	Y08 Y56	Y09 Y57	Y10 Y58	Y11 Y59	Y12 Y60	Y13 Y61	Y14 Y62	Y15 Y63	Y16 Y64	Y17 Y65	Y18 Y66	Y19 Y67	Y20 Y68	Y21 Y69	Y22 Y70	Y23 Y71	Y24 Y72	Y25 Y73	Y26 Y74	Y27 Y75	Y28 Y76	Y29 Y77	Y30 Y78	Y31 Y79	Y32 Y80	Y33 Y81	Y34 Y82	Y35 Y83	Y36 Y84	Y37 Y85	Y38 Y86	Y39 Y87	Y40 Y88	Y41 Y89	Y42 Y90	Y43 Y91	Y44 Y92	Y45 Y93	Y46 Y94	Y47 Y95	Y48 Y96	Y49 Y97	Y50 Y98	Y51 Y99	Y52 Y00	Y53 Y01	Y54 Y02	Y55 Y03	Y56 Y04	Y57 Y05	Y58 Y06	Y59 Y07	Y60 Y08	Y61 Y09	Y62 Y10	Y63 Y11	Y64 Y12	Y65 Y13	Y66 Y14	Y67 Y15	Y68 Y16	Y69 Y17	Y70 Y18	Y71 Y19	Y72 Y20	Y73 Y21	Y74 Y22	Y75 Y23	Y76 Y24	Y77 Y25	Y78 Y26	Y79 Y27	Y80 Y28	Y81 Y29	Y82 Y30	Y83 Y31	Y84 Y32	Y85 Y33	Y86 Y34	Y87 Y35	Y88 Y36	Y89 Y37	Y90 Y38	Y91 Y39	Y92 Y40	Y93 Y41	Y94 Y42	Y95 Y43	Y96 Y44	Y97 Y45	Y98 Y46	Y99 Y47
S1	X20 Y68	X21 Y69	X22 Y70	X23 Y71	X24 Y72	X25 Y73	X26 Y74	X27 Y75	X28 Y76	X29 Y77	X30 Y78	X31 Y79	X32 Y80	X33 Y81	X34 Y82	X35 Y83	X36 Y84	X37 Y85	X38 Y86	X39 Y87	X40 Y88	X41 Y89	X42 Y90	X43 Y91	X44 Y92	X45 Y93	X46 Y94	X47 Y95	X48 Y96	X49 Y97	X50 Y98	X51 Y99	X52 Y00	X53 Y01	X54 Y02	X55 Y03	X56 Y04	X57 Y05	X58 Y06	X59 Y07	X60 Y08	X61 Y09	X62 Y10	X63 Y11	X64 Y12	X65 Y13	X66 Y14	X67 Y15	X68 Y16	X69 Y17	X70 Y18	X71 Y19	X72 Y20	X73 Y21	X74 Y22	X75 Y23	X76 Y24	X77 Y25	X78 Y26	X79 Y27	X80 Y28	X81 Y29	X82 Y30	X83 Y31	X84 Y32	X85 Y33	X86 Y34	X87 Y35	X88 Y36	X89 Y37	X90 Y38	X91 Y39	X92 Y40	X93 Y41	X94 Y42	X95 Y43	X96 Y44	X97 Y45	X98 Y46	X99 Y47	Y00 Y48	Y01 Y49	Y02 Y50	Y03 Y51	Y04 Y52	Y05 Y53	Y06 Y54	Y07 Y55	Y08 Y56	Y09 Y57	Y10 Y58	Y11 Y59	Y12 Y60	Y13 Y61	Y14 Y62	Y15 Y63	Y16 Y64	Y17 Y65	Y18 Y66	Y19 Y67	Y20 Y68	Y21 Y69	Y22 Y70	Y23 Y71	Y24 Y72	Y25 Y73	Y26 Y74	Y27 Y75	Y28 Y76	Y29 Y77	Y30 Y78	Y31 Y79	Y32 Y80	Y33 Y81	Y34 Y82	Y35 Y83	Y36 Y84	Y37 Y85	Y38 Y86	Y39 Y87	Y40 Y88	Y41 Y89	Y42 Y90	Y43 Y91	Y44 Y92	Y45 Y93	Y46 Y94	Y47 Y95	Y48 Y96	Y49 Y97	Y50 Y98	Y51 Y99	Y52 Y00	Y53 Y01	Y54 Y02	Y55 Y03	Y56 Y04	Y57 Y05	Y58 Y06	Y59 Y07	Y60 Y08	Y61 Y09	Y62 Y10	Y63 Y11	Y64 Y12	Y65 Y13	Y66 Y14	Y67 Y15	Y68 Y16	Y69 Y17	Y70 Y18	Y71 Y19	Y72 Y20	Y73 Y21	Y74 Y22	Y75 Y23	Y76 Y24	Y77 Y25	Y78 Y26	Y79 Y27	Y80 Y28	Y81 Y29	Y82 Y30	Y83 Y31	Y84 Y32	Y85 Y33	Y86 Y34	Y87 Y35	Y88 Y36	Y89 Y37	Y90 Y38	Y91 Y39	Y92 Y40	Y93 Y41	Y94 Y42	Y95 Y43	Y96 Y44	Y97 Y45	Y98 Y46	Y99 Y47
S2	X20 Y68	X21 Y69	X22 Y70	X23 Y71	X24 Y72	X25 Y73	X26 Y74	X27 Y75	X28 Y76	X29 Y77	X30 Y78	X31 Y79	X32 Y80	X33 Y81	X34 Y82	X35 Y83	X36 Y84	X37 Y85	X38 Y86	X39 Y87	X40 Y88	X41 Y89	X42 Y90	X43 Y91	X44 Y92	X45 Y93	X46 Y94	X47 Y95	X48 Y96	X49 Y97	X50 Y98	X51 Y99	X52 Y00	X53 Y01	X54 Y02	X55 Y03	X56 Y04	X57 Y05	X58 Y06	X59 Y07	X60 Y08	X61 Y09	X62 Y10	X63 Y11	X64 Y12	X65 Y13	X66 Y14	X67 Y15	X68 Y16	X69 Y17	X70 Y18	X71 Y19	X72 Y20	X73 Y21	X74 Y22	X75 Y23	X76 Y24	X77 Y25	X78 Y26	X79 Y27	X80 Y28	X81 Y29	X82 Y30	X83 Y31	X84 Y32	X85 Y33	X86 Y34	X87 Y35	X88 Y36	X89 Y37	X90 Y38	X91 Y39	X92 Y40	X93 Y41	X94 Y42	X95 Y43	X96 Y44	X97 Y45	X98 Y46	X99 Y47	Y00 Y48	Y01 Y49	Y02 Y50	Y03 Y51	Y04 Y52	Y05 Y53	Y06 Y54	Y07 Y55	Y08 Y56	Y09 Y57	Y10 Y58	Y11 Y59	Y12 Y60	Y13 Y61	Y14 Y62	Y15 Y63	Y16 Y64	Y17 Y65	Y18 Y66	Y19 Y67	Y20 Y68	Y21 Y69	Y22 Y70	Y23 Y71	Y24 Y72	Y25 Y73	Y26 Y74	Y27 Y75	Y28 Y76	Y29 Y77	Y30 Y78	Y31 Y79	Y32 Y80	Y33 Y81	Y34 Y82	Y35 Y83	Y36 Y84	Y37 Y85	Y38 Y86	Y39 Y87	Y40 Y88	Y41 Y89	Y42 Y90	Y43 Y91	Y44 Y92	Y45 Y93	Y46 Y94	Y47 Y95	Y48 Y96	Y49 Y97	Y50 Y98	Y51 Y99	Y52 Y00	Y53 Y01	Y54 Y02	Y55 Y03	Y56 Y04	Y57 Y05	Y58 Y06	Y59 Y07	Y60 Y08	Y61 Y09	Y62 Y10	Y63 Y11	Y64 Y12	Y65 Y13	Y66 Y14	Y67 Y15	Y68 Y16	Y69 Y17	Y70 Y18	Y71 Y19	Y72 Y20	Y73 Y21	Y74 Y22	Y75 Y23	Y76 Y24	Y77 Y25	Y78 Y26	Y79 Y27	Y80 Y28	Y81 Y29	Y82 Y30	Y83 Y31	Y84 Y32	Y85 Y33	Y86 Y34	Y87 Y35	Y88 Y36	Y89 Y37	Y90 Y38	Y91 Y39	Y92 Y40	Y93 Y41	Y94 Y42	Y95 Y43	Y96 Y44	Y97 Y45	Y98 Y46	Y99 Y47
S3	X20 Y68	X21 Y69	X22 Y70	X23 Y71	X24 Y72	X25 Y73	X26 Y74	X27 Y75	X28 Y76	X29 Y77	X30 Y78	X31 Y79	X32 Y80	X33 Y81	X34 Y82	X35 Y83	X36 Y84	X37 Y85	X38 Y86	X39 Y87	X40 Y88	X41 Y89	X42 Y90	X43 Y91	X44 Y92	X45 Y93	X46 Y94	X47 Y95	X48 Y96	X49 Y97	X50 Y98	X51 Y99	X52 Y00	X53 Y01	X54 Y02	X55 Y03	X56 Y04	X57 Y05	X58 Y06	X59 Y07	X60 Y08	X61 Y09	X62 Y10	X63 Y11	X64 Y12	X65 Y13	X66 Y14	X67 Y15	X68 Y16	X69 Y17	X70 Y18	X71 Y19	X72 Y20	X73 Y21	X74 Y22	X75 Y23	X76 Y24	X77 Y25	X78 Y26	X79 Y27	X80 Y28	X81 Y29	X82 Y30	X83 Y31	X84 Y32	X85 Y33	X86 Y34	X87 Y35	X88 Y36	X89 Y37	X90 Y38	X91 Y39	X92 Y40	X93 Y41	X94 Y42	X95 Y43	X96 Y44	X97 Y45	X98 Y46	X99 Y47	Y00 Y48	Y01 Y49	Y02 Y50	Y03 Y51	Y04 Y52	Y05 Y53	Y06 Y54	Y07 Y55	Y08 Y56	Y09 Y57	Y10 Y58	Y11 Y59	Y12 Y60	Y13 Y61	Y14 Y62	Y15 Y63	Y16 Y64	Y17 Y65	Y18 Y66	Y19 Y67	Y20 Y68	Y21 Y69	Y22 Y70	Y23 Y71	Y24 Y72	Y25 Y73	Y26 Y74	Y27 Y75	Y28 Y76	Y29 Y77	Y30 Y78	Y31 Y79	Y32 Y80	Y33 Y81	Y34 Y82	Y35 Y83	Y36 Y84	Y37 Y85	Y38 Y86	Y39 Y87	Y40 Y88	Y41 Y89	Y42 Y90	Y43 Y91	Y44 Y92	Y45 Y93	Y46 Y94	Y47 Y95	Y48 Y96	Y49 Y97	Y50 Y98	Y51 Y99	Y52 Y00	Y53 Y01	Y54 Y02	Y55 Y03	Y56 Y04	Y57 Y05	Y58 Y06	Y59 Y07	Y60 Y08	Y61 Y09	Y62 Y10	Y63 Y11	Y64 Y12	Y65 Y13	Y66 Y14	Y67 Y15	Y68 Y16	Y69 Y17	Y70 Y18	Y71 Y19	Y72 Y20	Y73 Y21	Y74 Y22	Y75 Y23	Y76 Y24	Y77 Y25	Y78 Y26	Y79 Y27	Y80 Y28	Y81 Y29	Y82 Y30	Y83 Y31	Y84 Y32	Y85 Y33	Y86 Y34	Y87 Y35	Y88 Y36	Y89 Y37	Y90 Y38	Y91 Y39	Y92 Y40	Y93 Y41	Y94 Y42	Y95 Y43	Y96 Y44	Y97 Y45	Y98 Y46	Y99 Y47
S4	X20 Y68	X21 Y69	X22 Y70	X23 Y71	X24 Y72	X25 Y73	X26 Y74	X27 Y75	X28 Y76	X29 Y77	X30 Y78	X31 Y79	X32 Y80	X33 Y81	X34 Y82	X35 Y83	X36 Y84	X37 Y85	X38 Y86	X39 Y87	X40 Y88	X41 Y89	X42 Y90	X43 Y91	X44 Y92	X45 Y93	X46 Y94	X47 Y95	X48 Y96	X49 Y97	X50 Y98	X51 Y99	X52 Y00	X53 Y01	X54 Y02	X55 Y03	X56 Y04	X57 Y05	X58 Y06	X59 Y07	X60 Y08	X61 Y09	X62 Y10	X63 Y11	X64 Y12	X65 Y13	X66 Y14	X67 Y15	X68 Y16	X69 Y17	X70 Y18	X71 Y19	X72 Y20	X73 Y21	X74 Y22	X75 Y23	X76 Y24	X77 Y25	X78 Y26	X79 Y27	X80 Y28	X81 Y29	X82 Y30	X83 Y31	X84 Y32	X85 Y33	X86 Y34	X87 Y35	X88 Y36	X89 Y37	X90 Y38	X91 Y39	X92 Y40	X93 Y41	X94 Y42	X95 Y43	X96 Y44	X97 Y45	X98 Y46	X99 Y47	Y00 Y48	Y01 Y49	Y02 Y50	Y03 Y51	Y0																																																																																															

【図6】

本発明の第2の実施例の演算装置を説明するための図



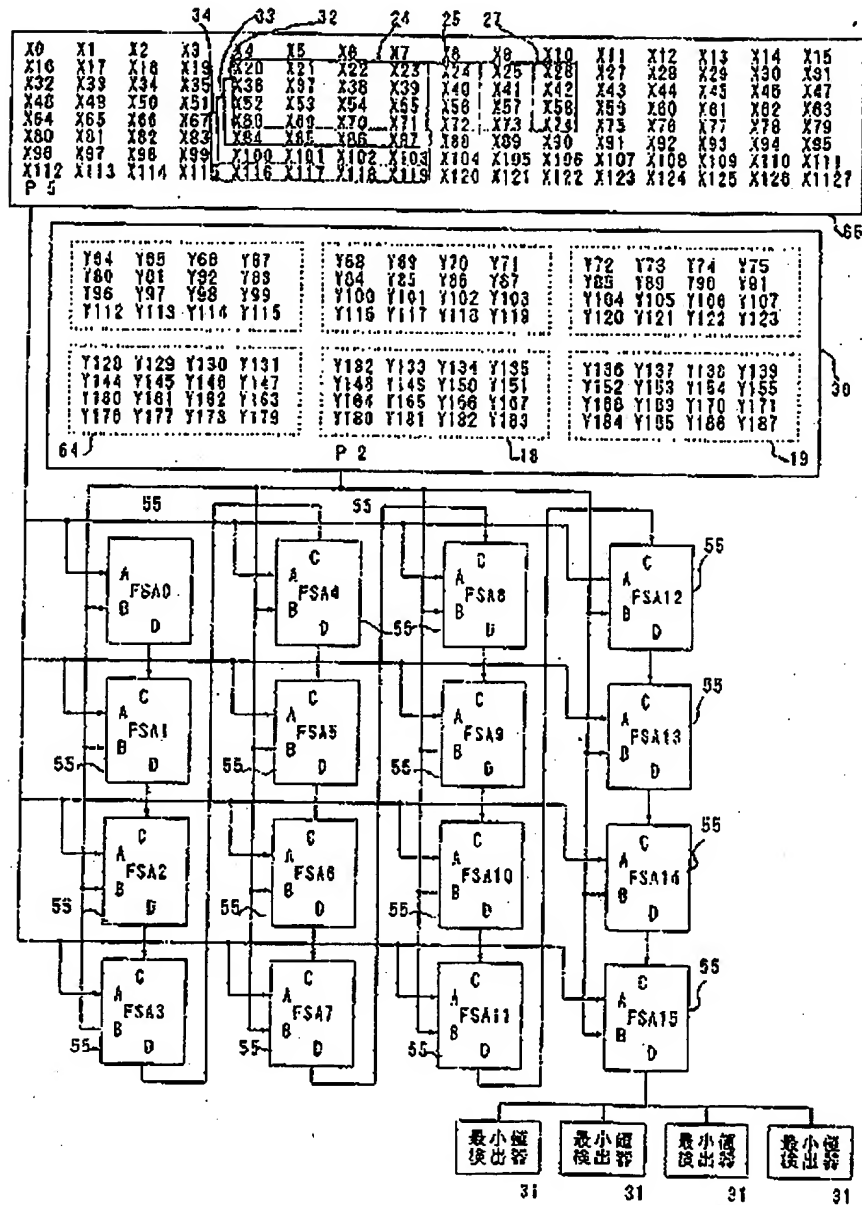
【図3】

本発明の第2の実施例の回路の流れを示す図

P0	X128	X21	X129	X22	X130	X23	X131	X24	X132	X25	X133	X26	X134	X27	X135	X28	X136	X29	X137	X30	X138	X31	X139	X32	X140	X33	X141	X34	X142	X35	X143	X36	X144	X37	X145	X38	X146	X39	X147	X40	X148	X41	X149	X42	X150	X43	X151	X44	X152	X45	X153	X46	X154	X47	X155	X48	X156	X49	X157	X50	X158	X51	X159	X52	X160	X53	X161	X54	X162	X55	X163	X56	X164	X57	X165	X58	X166	X59	X167	X60	X168	X61	X169	X62	X170	X63	X171	X64	X172	X65	X173	X66	X174	X67	X175	X68	X176	X69	X177	X70	X71	X72	X73	X74	X75	X76	X77	X78	X79	X80	X81	X82	X83	X84	X85	X86	X87	X88	X89	X90	X91	X92	X93	X94	X95	X96	X97	X98	X99	X100	X101	X102	X103	X104	X105	X106	X107	X108	X109	X110	X111	X112	X113	X114	X115	X116	X117	X118	X119	X120	X121	X122	X123	X124	X125	X126	X127	X128	X129	X130	X131	X132	X133	X134	X135	X136	X137	X138	X139	X140	X141	X142	X143	X144	X145	X146	X147	X148	X149	X150	X151	X152	X153	X154	X155	X156	X157	X158	X159	X160	X161	X162	X163	X164	X165	X166	X167	X168	X169	X170	X171	X172	X173	X174	X175	X176	X177	X178	X179	X180	X181	X182	X183	X184	X185	X186	X187	X188	X189	X190	X191	X192	X193	X194	X195	X196	X197	X198	X199	X200	X201	X202	X203	X204	X205	X206	X207	X208	X209	X210	X211	X212	X213	X214	X215	X216	X217	X218	X219	X220	X221	X222	X223	X224	X225	X226	X227	X228	X229	X230	X231	X232	X233	X234	X235	X236	X237	X238	X239	X240	X241	X242	X243	X244	X245	X246	X247	X248	X249	X250	X251	X252	X253	X254	X255	X256	X257	X258	X259	X260	X261	X262	X263	X264	X265	X266	X267	X268	X269	X270	X271	X272	X273	X274	X275	X276	X277	X278	X279	X280	X281	X282	X283	X284	X285	X286	X287	X288	X289	X290	X291	X292	X293	X294	X295	X296	X297	X298	X299	X300	X301	X302	X303	X304	X305	X306	X307	X308	X309	X310	X311	X312	X313	X314	X315	X316	X317	X318	X319	X320	X321	X322	X323	X324	X325	X326	X327	X328	X329	X330	X331	X332	X333	X334	X335	X336	X337	X338	X339	X340	X341	X342	X343	X344	X345	X346	X347	X348	X349	X350	X351	X352	X353	X354	X355	X356	X357	X358	X359	X360	X361	X362	X363	X364	X365	X366	X367	X368	X369	X370	X371	X372	X373	X374	X375	X376	X377	X378	X379	X380	X381	X382	X383	X384	X385	X386	X387	X388	X389	X390	X391	X392	X393	X394	X395	X396	X397	X398	X399	X400	X401	X402	X403	X404	X405	X406	X407	X408	X409	X410	X411	X412	X413	X414	X415	X416	X417	X418	X419	X420	X421	X422	X423	X424	X425	X426	X427	X428	X429	X430	X431	X432	X433	X434	X435	X436	X437	X438	X439	X440	X441	X442	X443	X444	X445	X446	X447	X448	X449	X450	X451	X452	X453	X454	X455	X456	X457	X458	X459	X460	X461	X462	X463	X464	X465	X466	X467	X468	X469	X470	X471	X472	X473	X474	X475	X476	X477	X478	X479	X480	X481	X482	X483	X484	X485	X486	X487	X488	X489	X490	X491	X492	X493	X494	X495	X496	X497	X498	X499	X500	X501	X502	X503	X504	X505	X506	X507	X508	X509	X510	X511	X512	X513	X514	X515	X516	X517	X518	X519	X520	X521	X522	X523	X524	X525	X526	X527	X528	X529	X530	X531	X532	X533	X534	X535	X536	X537	X538	X539	X540	X541	X542	X543	X544	X545	X546	X547	X548	X549	X550	X551	X552	X553	X554	X555	X556	X557	X558	X559	X560	X561	X562	X563	X564	X565	X566	X567	X568	X569	X570	X571	X572	X573	X574	X575	X576	X577	X578	X579	X580	X581	X582	X583	X584	X585	X586	X587	X588	X589	X590	X591	X592	X593	X594	X595	X596	X597	X598	X599	X600	X601	X602	X603	X604	X605	X606	X607	X608	X609	X610	X611	X612	X613	X614	X615	X616	X617	X618	X619	X620	X621	X622	X623	X624	X625	X626	X627	X628	X629	X630	X631	X632	X633	X634	X635	X636	X637	X638	X639	X640	X641	X642	X643	X644	X645	X646	X647	X648	X649	X650	X651	X652	X653	X654	X655	X656	X657	X658	X659	X660	X661	X662	X663	X664	X665	X666	X667	X668	X669	X670	X671	X672	X673	X674	X675	X676	X677	X678	X679	X680	X681	X682	X683	X684	X685	X686	X687	X688	X689	X690	X691	X692	X693	X694	X695	X696	X697	X698	X699	X700	X701	X702	X703	X704	X705	X706	X707	X708	X709	X710	X711	X712	X713	X714	X715	X716	X717	X718	X719	X720	X721	X722	X723	X724	X725	X726	X727	X728	X729	X730	X731	X732	X733	X734	X735	X736	X737	X738	X739	X740	X741	X742	X743	X744	X745	X746	X747	X748	X749	X750	X751	X752	X753	X754	X755	X756	X757	X758	X759	X760	X761	X762	X763	X764	X765	X766	X767	X768	X769	X770	X771	X772	X773	X774	X775	X776	X777	X778	X779	X780	X781	X782	X783	X784	X785	X786	X787	X788	X789	X790	X791	X792	X793	X794	X795	X796	X797	X798	X799	X800	X801	X802	X803	X804	X805	X806	X807	X808	X809	X810	X811	X812	X813	X814	X815	X816	X817	X818	X819	X820	X821	X822	X823	X824	X825	X826	X827	X828	X829	X830	X831	X832	X833	X834	X835	X836	X837	X838	X839	X840	X841	X842	X843	X844	X845	X846	X847	X848	X849	X850	X851	X852	X853	X854	X855	X856	X857	X858	X859	X860	X861	X862	X863	X864	X865	X866	X867	X868	X869	X870	X871	X872	X873	X874	X875	X876	X877	X878	X879	X880	X881	X882	X883	X884	X885	X886	X887	X888	X889	X890	X891	X892	X893	X894	X895	X896	X897	X898	X899	X900	X901	X902	X903	X904	X905	X906	X907	X908	X909	X910	X911	X912	X913	X914	X915	X916	X917	X918	X919	X920	X921	X922	X923	X924	X925	X926	X927	X928	X929	X930	X931	X932	X933	X934	X935	X936	X937	X938	X939	X940	X941	X942	X943	X944	X945	X946	X947	X948	X949	X950	X951	X952	X953	X954	X955	X956	X957	X958	X959	X960	X961	X962	X963	X964	X965	X966	X967	X968	X969	X970	X971	X972	X973	X974	X975	X976	X977	X978	X979	X980	X981	X982	X983	X984	X985	X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【図9】

本発明の第3の実施例の演算装置を説明するための図



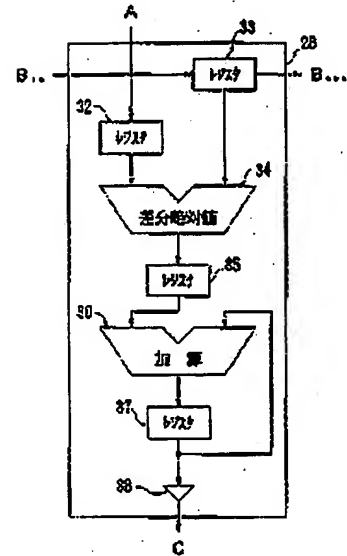
【図 10】

本発明の第 3 の実施例の画素の流れを示す図

P5	X120	X116	X121	X123	X118	X122	X131	X140	X144	X132	X135	X145	X139	X135	X146	X134	X130	X147
P2	173	1137	175	1133	176	1136	1133	178	1138	169	1153	179	1153	180	1154	181	1155	
FS40	120	1132	121	1133	122	1134	1131	123	1135	124	1136	125	1137	126	1138	127	1139	
FS41	128	1140	129	1141	130	1142	1139	131	1143	132	1144	133	1145	134	1146	135	1147	
FS42	136	1148	137	1149	138	1150	1147	139	1151	140	1152	141	1153	142	1154	143	1155	
FS43	144	1156	145	1157	146	1158	1155	147	1159	148	1160	149	1161	150	1162	151	1163	
FS44	152	1164	153	1165	154	1166	1163	155	1167	156	1168	157	1169	158	1170	159	1171	
FS45	160	1172	161	1173	162	1174	1171	163	1175	164	1176	165	1177	166	1178	167	1179	
FS46	168	1180	169	1181	170	1182	1179	171	1183	172	1184	173	1185	174	1186	175	1187	
FS47	176	1188	177	1189	178	1190	1187	179	1191	180	1192	181	1193	182	1194	183	1195	
FS48	184	1196	185	1197	186	1198	1195	187	1199	188	1200	189	1201	190	1202	191	1203	
FS49	192	1204	193	1205	194	1206	1203	195	1207	196	1208	197	1209	198	1210	199	1211	
FS50	200	1212	201	1213	202	1214	1211	203	1215	204	1216	205	1217	206	1218	207	1219	
FS51	208	1220	209	1221	210	1222	1219	211	1223	212	1224	213	1225	214	1226	215	1227	
FS52	216	1228	217	1229	218	1230	1227	219	1231	220	1232	221	1233	222	1234	223	1235	
FS53	224	1236	225	1237	226	1238	1235	227	1239	228	1240	229	1241	230	1242	231	1243	
FS54	232	1244	233	1245	234	1246	1243	235	1247	236	1248	237	1249	238	1250	239	1251	
FS55	240	1252	241	1253	242	1254	1251	243	1255	244	1256	245	1257	246	1258	247	1259	
FS56	248	1260	249	1261	250	1262	1259	251	1263	252	1264	253	1265	254	1266	255	1267	
FS57	256	1268	257	1269	258	1270	1267	259	1271	260	1272	261	1273	262	1274	263	1275	
FS58	264	1276	265	1277	266	1278	1275	267	1279	268	1280	269	1281	270	1282	271	1283	
FS59	272	1284	273	1285	274	1286	1283	275	1287	276	1288	277	1289	278	1290	279	1291	
FS60	280	1292	281	1293	282	1294	1291	283	1295	284	1296	285	1297	286	1298	287	1299	
FS61	288	1300	289	1301	290	1302	1299	291	1303	292	1304	293	1305	294	1306	295	1307	
FS62	296	1308	297	1309	298	1310	1307	299	1311	300	1312	301	1313	302	1314	303	1315	
FS63	304	1316	305	1317	306	1318	1315	307	1319	308	1320	309	1321	310	1322	311	1323	
FS64	312	1324	313	1325	314	1326	1323	315	1327	316	1328	317	1329	318	1330	319	1331	
FS65	320	1332	321	1333	322	1334	1331	323	1335	324	1336	325	1337	326	1338	327	1339	
FS66	328	1340	329	1341	330	1342	1339	331	1343	332	1344	333	1345	334	1346	335	1347	
FS67	336	1348	337	1349	338	1350	1347	339	1351	340	1352	341	1353	342	1354	343	1355	
FS68	344	1356	345	1357	346	1358	1355	347	1359	348	1360	349	1361	350	1362	351	1363	
FS69	352	1364	353	1365	354	1366	1363	355	1367	356	1368	357	1369	358	1370	359	1371	
FS70	360	1372	361	1373	362	1374	1371	363	1375	364	1376	365	1377	366	1378	367	1379	
FS71	368	1380	369	1381	370	1382	1379	371	1383	372	1384	373	1385	374	1386	375	1387	
FS72	376	1388	377	1389	378	1390	1387	379	1391	380	1392	381	1393	382	1394	383	1395	
FS73	384	1396	385	1397	386	1398	1395	387	1399	388	1400	389	1401	390	1402	391	1403	
FS74	392	1404	393	1405	394	1406	1403	395	1407	396	1408	397	1409	398	1410	399	1411	
FS75	400	1412	401	1413	402	1414	1411	403	1415	404	1416	405	1417	406	1418	407	1419	
FS76	408	1420	409	1421	410	1422	1419	411	1423	412	1424	413	1425	414	1426	415	1427	
FS77	416	1428	417	1429	418	1430	1427	419	1431	420	1432	421	1433	422	1434	423	1435	
FS78	424	1436	425	1437	426	1438	1435	427	1439	428	1440	429	1441	430	1442	431	1443	
FS79	432	1444	433	1445	434	1446	1443	435	1447	436	1448	437	1449	438	1450	439	1451	
FS80	440	1452	441	1453	442	1454	1451	443	1455	444	1456	445	1457	446	1458	447	1459	
FS81	448	1460	449	1461	450	1462	1459	451	1463	452	1464	453	1465	454	1466	455	1467	
FS82	456	1468	457	1469	458	1470	1467	459	1471	460	1472	461	1473	462	1474	463	1475	
FS83	464	1476	465	1477	466	1478	1475	467	1479	468	1480	469	1481	470	1482	471	1483	
FS84	472	1484	473	1485	474	1486	1483	475	1487	476	1488	477	1489	478	1490	479	1491	
FS85	480	1492	481	1493	482	1494	1491	483	1495	484	1496	485	1497	486	1498	487	1499	
FS86	488	1500	489	1501	490	1502	1499	491	1503	492	1504	493	1505	494	1506	495	1507	
FS87	496	1508	497	1509	498	1510	1507	499	1511	500	1512	501	1513	502	1514	503	1515	
FS88	504	1516	505	1517	506	1518	1515	507	1519	508	1520	509	1521	510	1522	511	1523	
FS89	512	1524	513	1525	514	1526	1523	515	1527	516	1528	517	1529	518	1530	519	1531	
FS90	520	1532	521	1533	522	1534	1531	523	1535	524	1536	525	1537	526	1538	527	1539	
FS91	528	1540	529	1541	530	1542	1539	531	1543	532	1544	533	1545	534	1546	535	1547	
FS92	536	1548	537	1549	538	1550	1547	539	1551	540	1552	541	1553	542	1554	543	1555	
FS93	544	1556	545	1557	546	1558	1555	547	1559	548	1560	549	1561	550	1562	551	1563	
FS94	552	1564	553	1565	554	1566	1563	555	1567	556	1568	557	1569	558	1570	559	1571	
FS95	560	1572	561	1573	562	1574	1571	563	1575	564	1576	565	1577	566	1578	567	1579	
FS96	568	1580	569	1581	570	1582	1579	571	1583	572	1584	573	1585	574	1586	575	1587	
FS97	576	1588	577	1589	578	1590	1587	579	1591	580	1592	581	1593	582	1594	583	1595	
FS98	584	1596	585	1597	586	1598	1595	587	1599	588	1600	589	1601	590	1602	591	1603	
FS99	592	1604	593	1605	594	1606	1603	595	1607	596	1608	597	1609	598	1610	599	1611	
FS00	596	1612	597	1613	598	1614	1611	599	1615	600	1616	601	1617	602	1618	603	1619	

【圖 17】

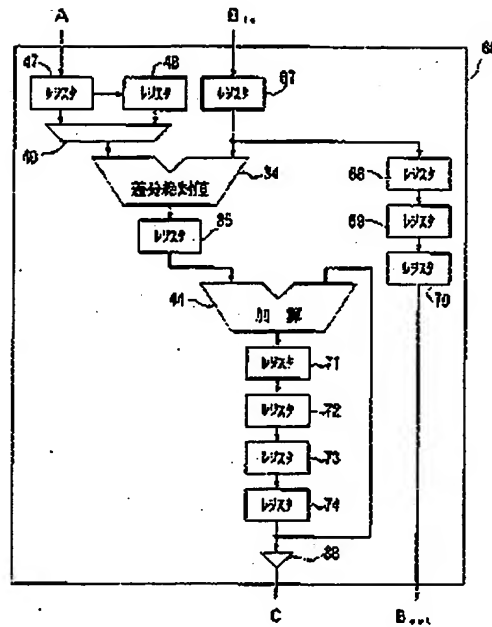
### 従来の技術の第 1 の例の演算器の構成図





【図11】

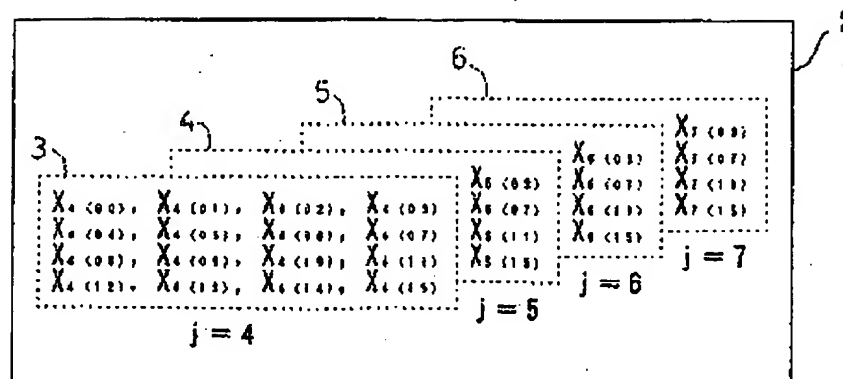
本発明の第4の実施例の演算器の構成図



【図13】

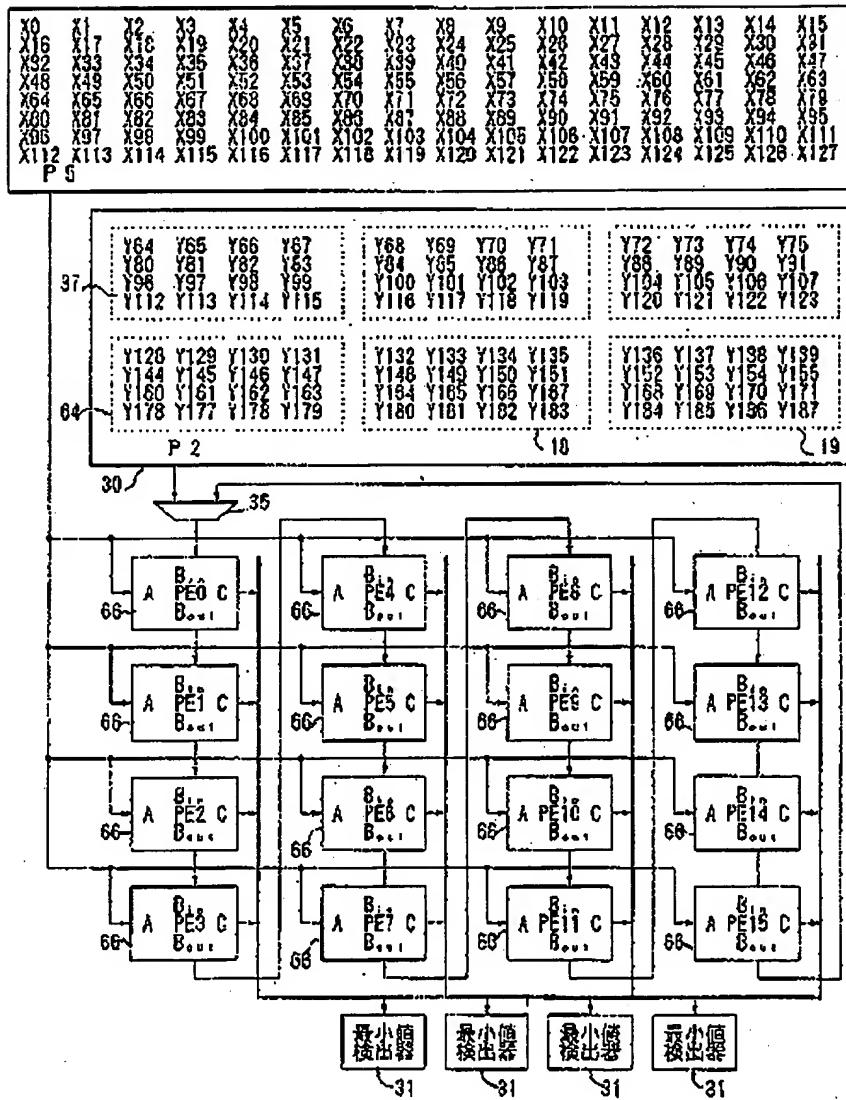
動き補償演算の対象となる被探索画素ブロックとテンプレート

Y (0 0)	Y (0 1)	Y (0 2)	Y (0 3)
Y (0 4)	Y (0 5)	Y (0 6)	Y (0 7)
Y (0 8)	Y (0 9)	Y (1 0)	Y (1 1)
Y (1 2)	Y (1 3)	Y (1 4)	Y (1 5)



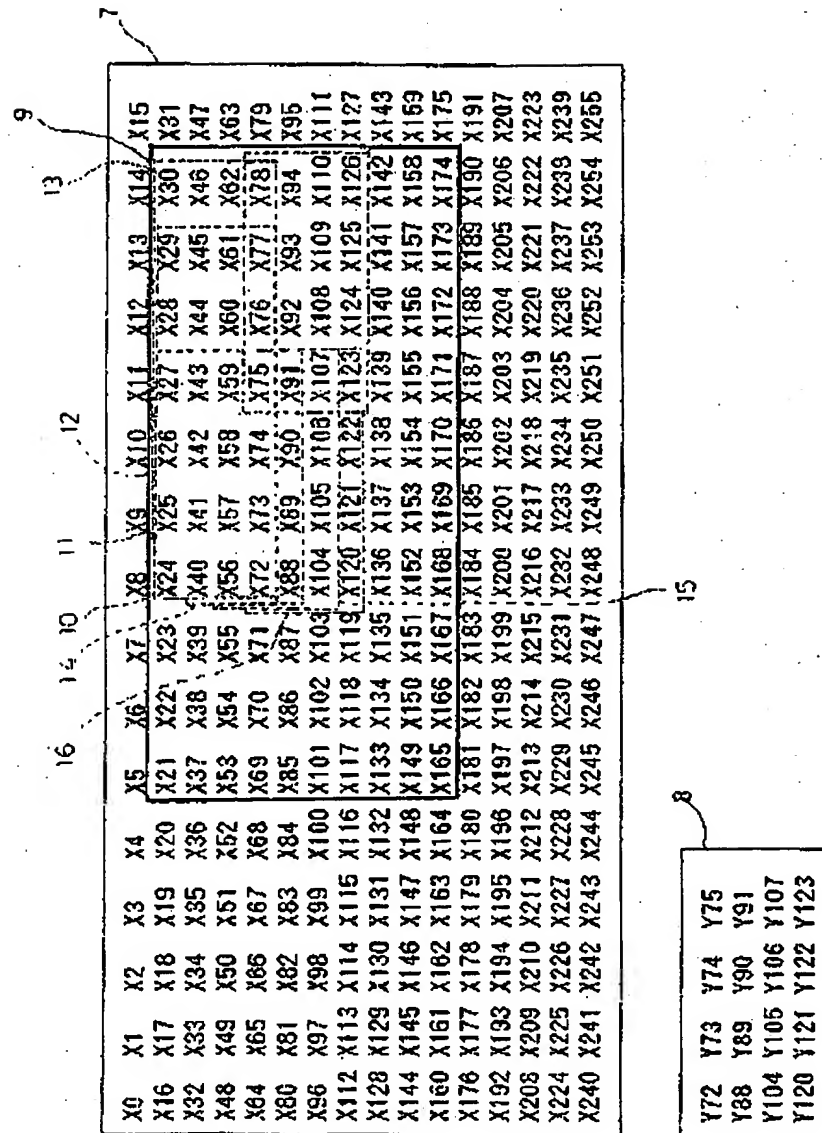
【図12】

本発明の第4の実施例の演算装置を説明するための図



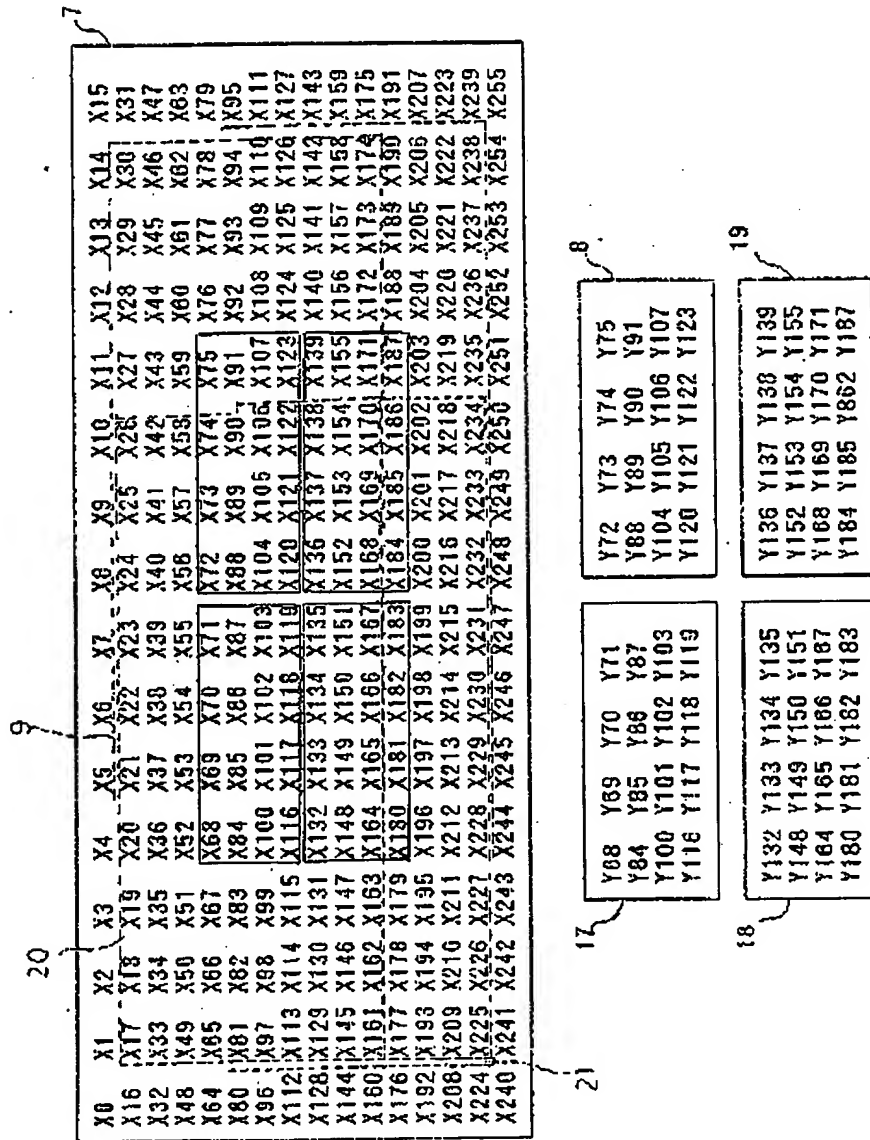
【図14】

被探索ブロック間の隣りを示す図



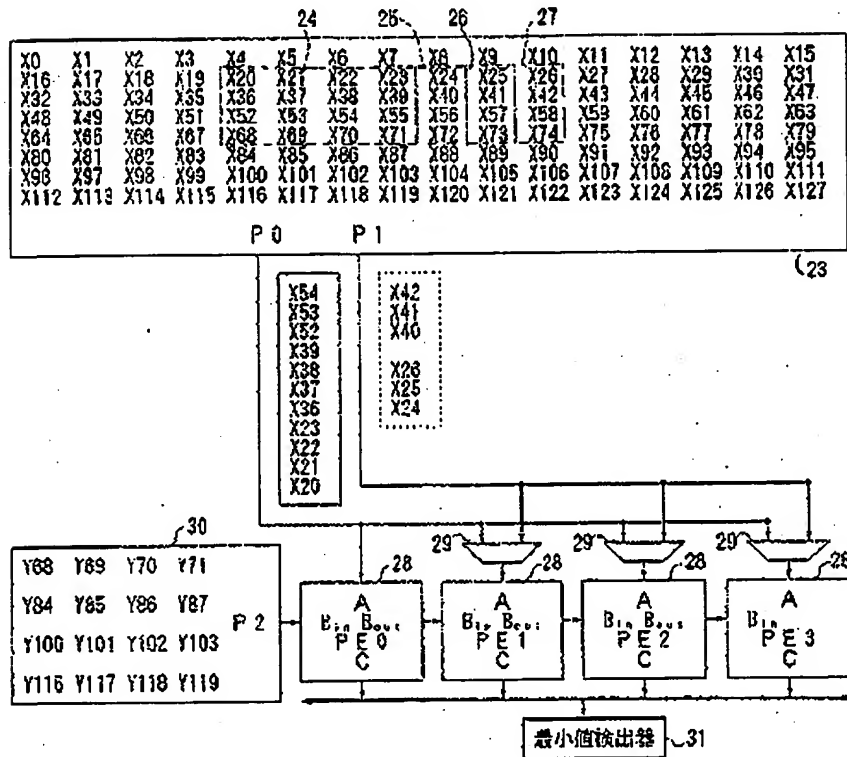
[図15]

接続したテンプレートに対する探索領域の画なりを示す図



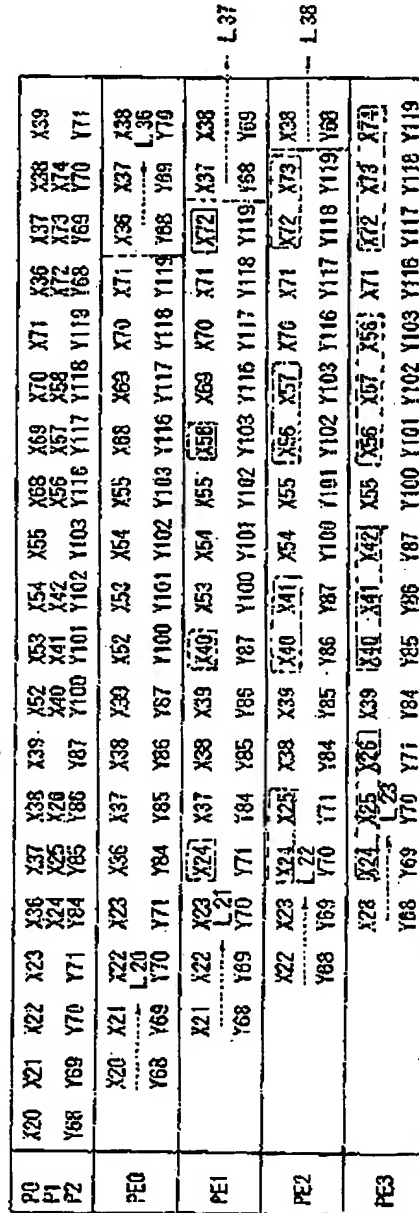
【図16】

動き補償を全探索法で計算する従来技術の第1の例の  
装置を説明するための図



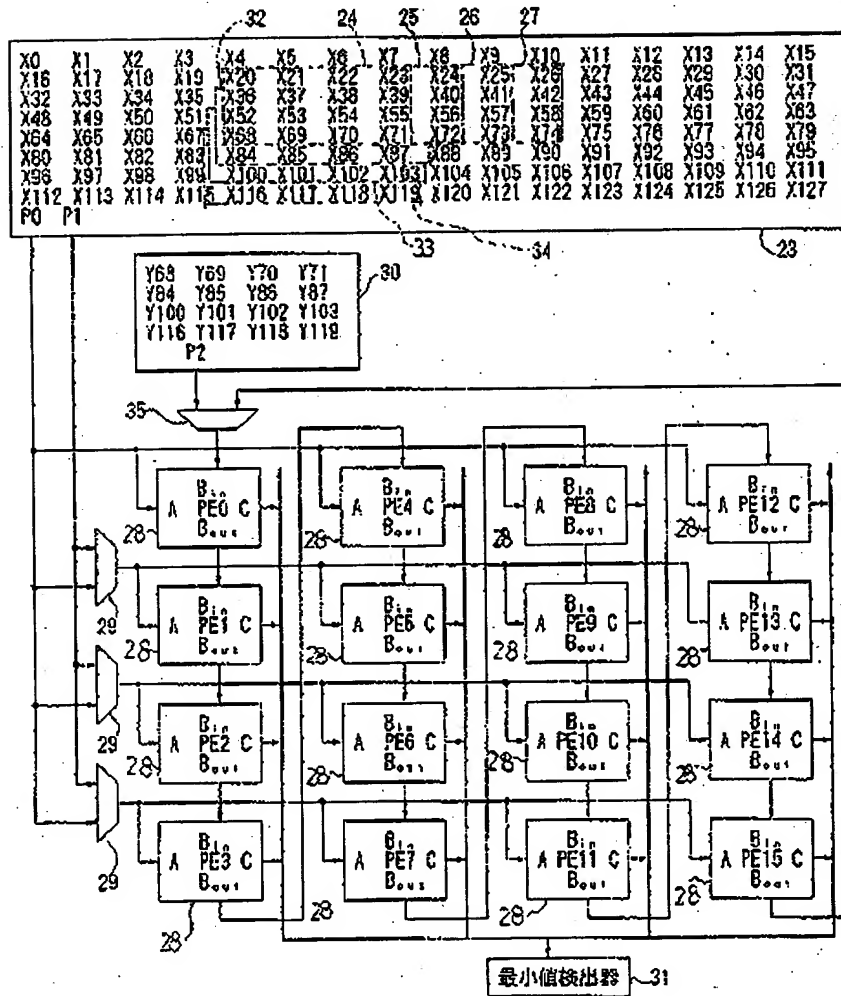
【図18】

従来技術の第1の例における画素の流れを示す図



【図19】

動き補償を全探索法で計算する従来の第2の例の装置を説明するための図



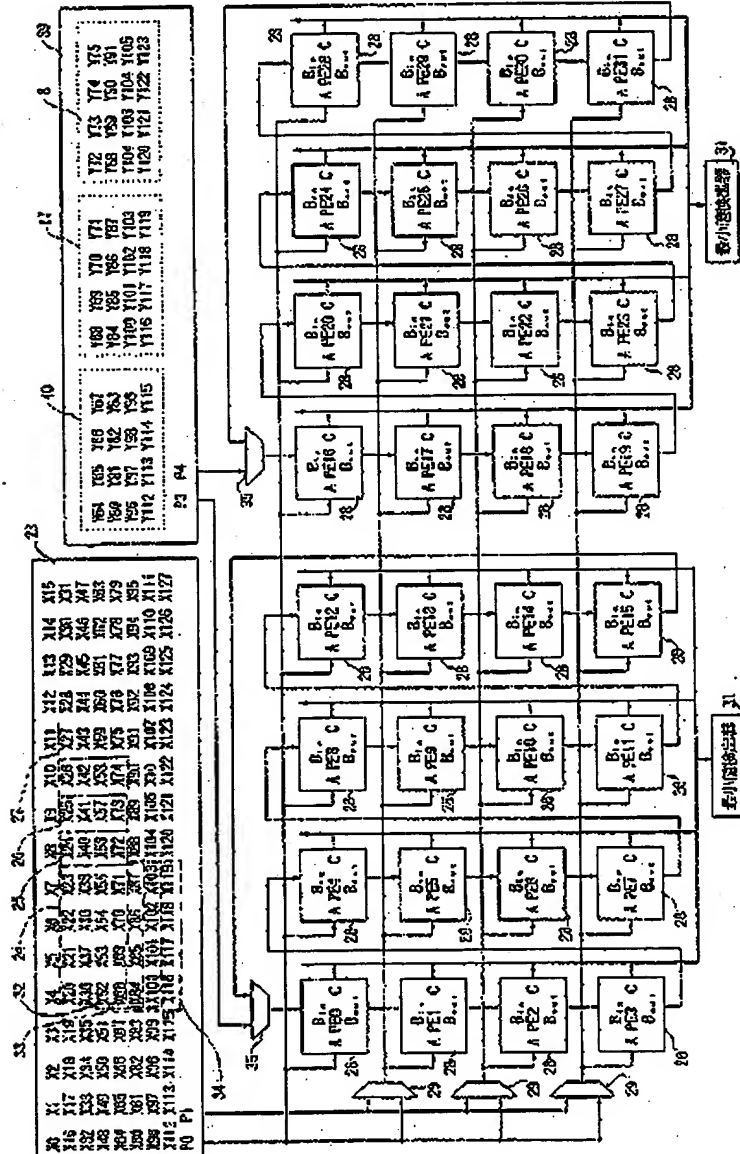
従来技術の第2の例における画素の流れを示す図

P0	X20	X21	X22	X23	X24	X25	X26	X27	X28	X29	X30	X31	X32	X33	X34	X35	X36	X37	X38	X39	X40	X41	X42	X43	X44	X45	X46	X47	X48	X49	X50	X51	X52	X53	X54	X55	X56	X57	X58	X59	X60	X61	X62	X63	X64	X65	X66	X67	X68	X69	X70	X71	X72	X73	X74	X75	X76	X77	X78	X79	X80	X81	X82	X83	X84	X85	X86	X87	X88	X89	X90	X91	X92	X93	X94	X95	X96	X97	X98	X99	X100	X101	X102	X103	X104	X105	X106	X107	X108	X109	X110	X111	X112	X113	X114	X115	X116	X117	X118	X119	X120	X121	X122	X123	X124	X125	X126	X127	X128	X129	X130	X131	X132	X133	X134	X135	X136	X137	X138	X139	X140	X141	X142	X143	X144	X145	X146	X147	X148	X149	X150	X151	X152	X153	X154	X155	X156	X157	X158	X159	X160	X161	X162	X163	X164	X165	X166	X167	X168	X169	X170	X171	X172	X173	X174	X175	X176	X177	X178	X179	X180	X181	X182	X183	X184	X185	X186	X187	X188	X189	X190	X191	X192	X193	X194	X195	X196	X197	X198	X199	X200	X201	X202	X203	X204	X205	X206	X207	X208	X209	X210	X211	X212	X213	X214	X215	X216	X217	X218	X219	X220	X221	X222	X223	X224	X225	X226	X227	X228	X229	X230	X231	X232	X233	X234	X235	X236	X237	X238	X239	X240	X241	X242	X243	X244	X245	X246	X247	X248	X249	X250	X251	X252	X253	X254	X255	X256	X257	X258	X259	X260	X261	X262	X263	X264	X265	X266	X267	X268	X269	X270	X271	X272	X273	X274	X275	X276	X277	X278	X279	X280	X281	X282	X283	X284	X285	X286	X287	X288	X289	X290	X291	X292	X293	X294	X295	X296	X297	X298	X299	X300	X301	X302	X303	X304	X305	X306	X307	X308	X309	X310	X311	X312	X313	X314	X315	X316	X317	X318	X319	X320	X321	X322	X323	X324	X325	X326	X327	X328	X329	X330	X331	X332	X333	X334	X335	X336	X337	X338	X339	X340	X341	X342	X343	X344	X345	X346	X347	X348	X349	X350	X351	X352	X353	X354	X355	X356	X357	X358	X359	X360	X361	X362	X363	X364	X365	X366	X367	X368	X369	X370	X371	X372	X373	X374	X375	X376	X377	X378	X379	X380	X381	X382	X383	X384	X385	X386	X387	X388	X389	X390	X391	X392	X393	X394	X395	X396	X397	X398	X399	X400	X401	X402	X403	X404	X405	X406	X407	X408	X409	X410	X411	X412	X413	X414	X415	X416	X417	X418	X419	X420	X421	X422	X423	X424	X425	X426	X427	X428	X429	X430	X431	X432	X433	X434	X435	X436	X437	X438	X439	X440	X441	X442	X443	X444	X445	X446	X447	X448	X449	X450	X451	X452	X453	X454	X455	X456	X457	X458	X459	X460	X461	X462	X463	X464	X465	X466	X467	X468	X469	X470	X471	X472	X473	X474	X475	X476	X477	X478	X479	X480	X481	X482	X483	X484	X485	X486	X487	X488	X489	X490	X491	X492	X493	X494	X495	X496	X497	X498	X499	X500	X501	X502	X503	X504	X505	X506	X507	X508	X509	X510	X511	X512	X513	X514	X515	X516	X517	X518	X519	X520	X521	X522	X523	X524	X525	X526	X527	X528	X529	X530	X531	X532	X533	X534	X535	X536	X537	X538	X539	X540	X541	X542	X543	X544	X545	X546	X547	X548	X549	X550	X551	X552	X553	X554	X555	X556	X557	X558	X559	X560	X561	X562	X563	X564	X565	X566	X567	X568	X569	X570	X571	X572	X573	X574	X575	X576	X577	X578	X579	X580	X581	X582	X583	X584	X585	X586	X587	X588	X589	X590	X591	X592	X593	X594	X595	X596	X597	X598	X599	X600	X601	X602	X603	X604	X605	X606	X607	X608	X609	X610	X611	X612	X613	X614	X615	X616	X617	X618	X619	X620	X621	X622	X623	X624	X625	X626	X627	X628	X629	X630	X631	X632	X633	X634	X635	X636	X637	X638	X639	X640	X641	X642	X643	X644	X645	X646	X647	X648	X649	X650	X651	X652	X653	X654	X655	X656	X657	X658	X659	X660	X661	X662	X663	X664	X665	X666	X667	X668	X669	X670	X671	X672	X673	X674	X675	X676	X677	X678	X679	X680	X681	X682	X683	X684	X685	X686	X687	X688	X689	X690	X691	X692	X693	X694	X695	X696	X697	X698	X699	X700	X701	X702	X703	X704	X705	X706	X707	X708	X709	X710	X711	X712	X713	X714	X715	X716	X717	X718	X719	X720	X721	X722	X723	X724	X725	X726	X727	X728	X729	X730	X731	X732	X733	X734	X735	X736	X737	X738	X739	X740	X741	X742	X743	X744	X745	X746	X747	X748	X749	X750	X751	X752	X753	X754	X755	X756	X757	X758	X759	X760	X761	X762	X763	X764	X765	X766	X767	X768	X769	X770	X771	X772	X773	X774	X775	X776	X777	X778	X779	X780	X781	X782	X783	X784	X785	X786	X787	X788	X789	X790	X791	X792	X793	X794	X795	X796	X797	X798	X799	X800	X801	X802	X803	X804	X805	X806	X807	X808	X809	X810	X811	X812	X813	X814	X815	X816	X817	X818	X819	X820	X821	X822	X823	X824	X825	X826	X827	X828	X829	X830	X831	X832	X833	X834	X835	X836	X837	X838	X839	X840	X841	X842	X843	X844	X845	X846	X847	X848	X849	X850	X851	X852	X853	X854	X855	X856	X857	X858	X859	X860	X861	X862	X863	X864	X865	X866	X867	X868	X869	X870	X871	X872	X873	X874	X875	X876	X877	X878	X879	X880	X881	X882	X883	X884	X885	X886	X887	X888	X889	X890	X891	X892	X893	X894	X895	X896	X897	X898	X899	X900	X901	X902	X903	X904	X905	X906	X907	X908	X909	X910	X911	X912	X913	X914	X915	X916	X917	X918	X919	X920	X921	X922	X923	X924	X925	X926	X927	X928	X929	X930	X931	X932	X933	X934	X935	X936	X937	X938	X939	X940	X941	X942	X943	X944	X945	X946	X947	X948	X949	X950	X951	X952	X953	X954	X955	X956	X957	X958	X959	X960	X961	X962	X963	X964	X965	X966	X967	X968	X969	X970	X971	X972	X973	X974	X975	X976	X977	X978	X979	X980	X981	X982	X983	X984	X985	X986	X987	X988	X989	X990	X991	X992	X993	X994	X995	X996	X997	X998	X999	X1000	X1001	X1002	X1003	X1004	X1005	X1006	X1007	X1008	X1009	X1010	X1011	X1012	X1013	X1014	X1015	X1016	X1017	X1018	X1019	X1020	X1021	X1022	X1023	X1024	X1025	X1026	X1027	X1028	X1029	X1030	X1031	X1032	X1033	X1034	X1035	X1036	X1037	X1038	X1039	X1040	X1041	X1042	X1043	X1044	X1045	X1046	X1047	X1048	X1049	X1050	X1051	X1052	X1053	X1054	X1055	X1056	X1057	X1058	X1059	X1060	X1061	X1062	X1063	X1064	X1065	X1066	X1067	X1068	X1069	X1070	X1071	X1072	X1073	X1074	X1075	X1076	X1077	X1078	X1079	X1080	X1081	X1082	X1083	X1084	X1085	X1086	X1087	X1088	X1089	X1090	X1091	X1092	X1093	X1094	X1095	X1096	X1097	X1098	X1099	X1100	X1101	X1102	X1103	X1104	X1105	X1106	X1107	X1108	X1109	X1110	X1111	X1112	X1113	X1114	X1115	X1116	X1117	X1118	X1119	X1120	X1121	X1122	X1123	X1124	X1125	X1126	X1127	X1128	X1129	X1130	X1131	X1132	X1133	X1134	X1135	X1136	X1137	X1138	X1139	X1140	X1141	X1142	X1143	X1144	X1145	X1146	X1147	X1148	X1149	X1150	X1151	X1152	X1153	X1154	X1155	X1156	X1157	X1158	X1159	X1160	X1161	X1162	X1163	X1164	X1165	X1166	X1167	X1168	X1169	X1170	X1171	X1172	X1173	X1174	X1175	X1176	X1177	X1178	X1179	X1180	X1181	X1182	X1183	X1184	X1185	X1186	X1187	X1188	X1189	X1190	X1191	X1192	X1193	X1194	X1195	X1196	X1197	X1198	X1199	X1200	X1201	X1202	X1203	X1204	X1205	X1206	X1207	X1208	X1209	X1210	X1211	X1212	X1213	X1214	X1215	X1216	X1217	X1218	X1219	X1220	X1221	X1222	X1223	X1224	X1225	X1226	X1227	X1228	X1229	X1230	X1231	X1232	X1233	X1234	X1235	X1236	X1237	X1238	X1239	X1240	X1241	X1242	X1243	X1244	X1245	X1246	X1247	X1248	X1249	X1250	X1251	X1252	X1253	X1254	X1255	X1256	X1257	X1258	X1259	X1260	X1261	X1262	X1263	X1264	X1265	X1266	X1267	X1268	X1269	X1270	X1271	X1272	X1273	X1274	X1275	X1276	X1277	X1278	X1279	X1280	X1281	X1282	X1283	X1284	X1285	X1286	X1287	X1288	X1289	X1290	X1291	X1292	X1293	X1294	X1295	X1296	X1297	X1298	X1299	X1300	X1301	X1302	X1303	X1304	X1305	X1306	X1307	X1308	X1309	X1310	X1311	X1312	X1313	X1314	X1315	X1316	X1317	X1318	X1319	X1320	X1321	X1322	X1323	X1324	X1325	X1326	X1327	X1328	X1329	X1330	X1331	X1332	X1333	X1334	X1335	X1336	X1337	X1338	X1339	X1340	X1341	X1342	X1343	X1344	X1345	X1346	X1347	X1348	X1349	X1350	X1351	X1352	X1353	X1354	X1355	X1356	X1357	X1358	X1359	X1360	X1361	X1362	X1363	X1364	X1365	X1366	X1367	X1368	X1369	X1370	X1371	X1372	X1373	X1374	X1375	X1376	X1377	X1378	X1379	X1380	X1381	X1382	X1383	X1384	X1385	X1386	X1387	X1388	X1389	X1390	X1391	X1392	X1393	X1394	X1395	X1396	X1397	X1398	X1399	X1400	X1401	X1402	X1403	X1404	X1405	X1406	X1407	X1408	X1409	X1410	X1411	X1412	X1413	X1414	X1415	X1416	X1417	X1418	X1419	X1420	X1421	X1422	X1423	X1424	X1425	X1426	X1427	X1428	X1429	X1430	X1431	X1432	X1433	X1434	X1435	X1436	X1437	X1438	X1439	X1440	X1441	X1442	X1443	X1444	X1445	X1446	X1447	X1448	X1449	X1450	X1451	X1452	X1453	X1454	X1455	X1456	X1457	X1458	X1459	X1460	X1461	X1462	X1463	X1464	X1465	X1466	X1467	X1468	X1469	X1470	X1471	X1472	X1473	X1474	X1475	X1476	X1477	X1478	X1479	X1480	X1481	X1482	X1483	X1484	X1485	X1486	X1487	X1488	X1489	X1490	X1491	X1492	X1493	X1494	X1495	X1496	X1497	X1498	X1499	X1500	X1501	X1502	X1503	X1504	X1505	X1506	X1507	X1508	X1509	X1510	X1511	X1512
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【図21】

動画像を全探索法で計算する従来技術の第3の例の  
 装置を説明するための図



【図22】

従来技術の第3の例における要素の流れを示す図

P0	X20	X21	X22	X23	X24	X25	X26	X27	X28	X29	X30	X31	X32	X33	X34	X35	X36	X37	X38	X39	X40	X41	X42	X43	X44	X45	X46	X47	X48	X49	X50	X51	X52	X53	X54	X55	X56	X57	X58	X59	X60	X61	X62	X63	X64	X65	X66	X67	X68	X69	X70	X71	X72	X73	X74	X75	X76	X77	X78	X79	X80	X81	X82	X83	X84	X85	X86	X87	X88	X89	X90	X91	X92	X93	X94	X95	X96	X97	X98	X99	X100	X101	X102	X103	X104	X105	X106	X107	X108	X109	X110	X111	X112	X113	X114	X115	X116	X117	X118	X119	X120	X121	X122	X123	X124	X125	X126	X127	X128	X129	X130	X131	X132	X133	X134	X135	X136	X137	X138	X139	X140	X141	X142	X143	X144	X145	X146	X147	X148	X149	X150	X151	X152	X153	X154	X155	X156	X157	X158	X159	X160	X161	X162	X163	X164	X165	X166	X167	X168	X169	X170	X171	X172	X173	X174	X175	X176	X177	X178	X179	X180	X181	X182	X183	X184	X185	X186	X187	X188	X189	X190	X191	X192	X193	X194	X195	X196	X197	X198	X199	X200	X201	X202	X203	X204	X205	X206	X207	X208	X209	X210	X211	X212	X213	X214	X215	X216	X217	X218	X219	X220	X221	X222	X223	X224	X225	X226	X227	X228	X229	X230	X231	X232	X233	X234	X235	X236	X237	X238	X239	X240	X241	X242	X243	X244	X245	X246	X247	X248	X249	X250	X251	X252	X253	X254	X255	X256	X257	X258	X259	X260	X261	X262	X263	X264	X265	X266	X267	X268	X269	X270	X271	X272	X273	X274	X275	X276	X277	X278	X279	X280	X281	X282	X283	X284	X285	X286	X287	X288	X289	X290	X291	X292	X293	X294	X295	X296	X297	X298	X299	X300	X301	X302	X303	X304	X305	X306	X307	X308	X309	X310	X311	X312	X313	X314	X315	X316	X317	X318	X319	X320	X321	X322	X323	X324	X325	X326	X327	X328	X329	X330	X331	X332	X333	X334	X335	X336	X337	X338	X339	X340	X341	X342	X343	X344	X345	X346	X347	X348	X349	X350	X351	X352	X353	X354	X355	X356	X357	X358	X359	X360	X361	X362	X363	X364	X365	X366	X367	X368	X369	X370	X371	X372	X373	X374	X375	X376	X377	X378	X379	X380	X381	X382	X383	X384	X385	X386	X387	X388	X389	X390	X391	X392	X393	X394	X395	X396	X397	X398	X399	X400	X401	X402	X403	X404	X405	X406	X407	X408	X409	X410	X411	X412	X413	X414	X415	X416	X417	X418	X419	X420	X421	X422	X423	X424	X425	X426	X427	X428	X429	X430	X431	X432	X433	X434	X435	X436	X437	X438	X439	X440	X441	X442	X443	X444	X445	X446	X447	X448	X449	X450	X451	X452	X453	X454	X455	X456	X457	X458	X459	X460	X461	X462	X463	X464	X465	X466	X467	X468	X469	X470	X471	X472	X473	X474	X475	X476	X477	X478	X479	X480	X481	X482	X483	X484	X485	X486	X487	X488	X489	X490	X491	X492	X493	X494	X495	X496	X497	X498	X499	X500	X501	X502	X503	X504	X505	X506	X507	X508	X509	X510	X511	X512	X513	X514	X515	X516	X517	X518	X519	X520	X521	X522	X523	X524	X525	X526	X527	X528	X529	X530	X531	X532	X533	X534	X535	X536	X537	X538	X539	X540	X541	X542	X543	X544	X545	X546	X547	X548	X549	X550	X551	X552	X553	X554	X555	X556	X557	X558	X559	X560	X561	X562	X563	X564	X565	X566	X567	X568	X569	X570	X571	X572	X573	X574	X575	X576	X577	X578	X579	X580	X581	X582	X583	X584	X585	X586	X587	X588	X589	X590	X591	X592	X593	X594	X595	X596	X597	X598	X599	X600	X601	X602	X603	X604	X605	X606	X607	X608	X609	X610	X611	X612	X613	X614	X615	X616	X617	X618	X619	X620	X621	X622	X623	X624	X625	X626	X627	X628	X629	X630	X631	X632	X633	X634	X635	X636	X637	X638	X639	X640	X641	X642	X643	X644	X645	X646	X647	X648	X649	X650	X651	X652	X653	X654	X655	X656	X657	X658	X659	X660	X661	X662	X663	X664	X665	X666	X667	X668	X669	X670	X671	X672	X673	X674	X675	X676	X677	X678	X679	X680	X681	X682	X683	X684	X685	X686	X687	X688	X689	X690	X691	X692	X693	X694	X695	X696	X697	X698	X699	X700	X701	X702	X703	X704	X705	X706	X707	X708	X709	X710	X711	X712	X713	X714	X715	X716	X717	X718	X719	X720	X721	X722	X723	X724	X725	X726	X727	X728	X729	X730	X731	X732	X733	X734	X735	X736	X737	X738	X739	X740	X741	X742	X743	X744	X745	X746	X747	X748	X749	X750	X751	X752	X753	X754	X755	X756	X757	X758	X759	X760	X761	X762	X763	X764	X765	X766	X767	X768	X769	X770	X771	X772	X773	X774	X775	X776	X777	X778	X779	X780	X781	X782	X783	X784	X785	X786	X787	X788	X789	X790	X791	X792	X793	X794	X795	X796	X797	X798	X799	X800	X801	X802	X803	X804	X805	X806	X807	X808	X809	X810	X811	X812	X813	X814	X815	X816	X817	X818	X819	X820	X821	X822	X823	X824	X825	X826	X827	X828	X829	X830	X831	X832	X833	X834	X835	X836	X837	X838	X839	X840	X841	X842	X843	X844	X845	X846	X847	X848	X849	X850	X851	X852	X853	X854	X855	X856	X857	X858	X859	X860	X861	X862	X863	X864	X865	X866	X867	X868	X869	X870	X871	X872	X873	X874	X875	X876	X877	X878	X879	X880	X881	X882	X883	X884	X885	X886	X887	X888	X889	X890	X891	X892	X893	X894	X895	X896	X897	X898	X899	X900	X901	X902	X903	X904	X905	X906	X907	X908	X909	X910	X911	X912	X913	X914	X915	X916	X917	X918	X919	X920	X921	X922	X923	X924	X925	X926	X927	X928	X929	X930	X931	X932	X933	X934	X935	X936	X937	X938	X939	X940	X941	X942	X943	X944	X945	X946	X947	X948	X949	X950	X951	X952	X953	X954	X955	X956	X957	X958	X959	X960	X961	X962	X963	X964	X965	X966	X967	X968	X969	X970	X971	X972	X973	X974	X975	X976	X977	X978	X979	X980	X981	X982	X983	X984	X985	X986	X987	X988	X989	X990	X991	X992	X993	X994	X995	X996	X997	X998	X999	X1000	X1001	X1002	X1003	X1004	X1005	X1006	X1007	X1008	X1009	X1010	X1011	X1012	X1013	X1014	X1015	X1016	X1017	X1018	X1019	X1020	X1021	X1022	X1023	X1024	X1025	X1026	X1027	X1028	X1029	X1030	X1031	X1032	X1033	X1034	X1035	X1036	X1037	X1038	X1039	X1040	X1041	X1042	X1043	X1044	X1045	X1046	X1047	X1048	X1049	X1050	X1051	X1052	X1053	X1054	X1055	X1056	X1057	X1058	X1059	X1060	X1061	X1062	X1063	X1064	X1065	X1066	X1067	X1068	X1069	X1070	X1071	X1072	X1073	X1074	X1075	X1076	X1077	X1078	X1079	X1080	X1081	X1082	X1083	X1084	X1085	X1086	X1087	X1088	X1089	X1090	X1091	X1092	X1093	X1094	X1095	X1096	X1097	X1098	X1099	X1100	X1101	X1102	X1103	X1104	X1105	X1106	X1107	X1108	X1109	X1110	X1111	X1112	X1113	X1114	X1115	X1116	X1117	X1118	X1119	X1120	X1121	X1122	X1123	X1124	X1125	X1126	X1127	X1128	X1129	X1130	X1131	X1132	X1133	X1134	X1135	X1136	X1137	X1138	X1139	X1140	X1141	X1142	X1143	X1144	X1145	X1146	X1147	X1148	X1149	X1150	X1151	X1152	X1153	X1154	X1155	X1156	X1157	X1158	X1159	X1160	X1161	X1162	X1163	X1164	X1165	X1166	X1167	X1168	X1169	X1170	X1171	X1172	X1173	X1174	X1175	X1176	X1177	X1178	X1179	X1180	X1181	X1182	X1183	X1184	X1185	X1186	X1187	X1188	X1189	X1190	X1191	X1192	X1193	X1194	X1195	X1196	X1197	X1198	X1199	X1200	X1201	X1202	X1203	X1204	X1205	X1206	X1207	X1208	X1209	X1210	X1211	X1212	X1213	X1214	X1215	X1216	X1217	X1218	X1219	X1220	X1221	X1222	X1223	X1224	X1225	X1226	X1227	X1228	X1229	X1230	X1231	X1232	X1233	X1234	X1235	X1236	X1237	X1238	X1239	X1240	X1241	X1242	X1243	X1244	X1245	X1246	X1247	X1248	X1249	X1250	X1251	X1252	X1253	X1254	X1255	X1256	X1257	X1258	X1259	X1260	X1261	X1262	X1263	X1264	X1265	X1266	X1267	X1268	X1269	X1270	X1271	X1272	X1273	X1274	X1275	X1276	X1277	X1278	X1279	X1280	X1281	X1282	X1283	X1284	X1285	X1286	X1287	X1288	X1289	X1290	X1291	X1292	X1293	X1294	X1295	X1296	X1297	X1298	X1299	X1300	X1301	X1302	X1303	X1304	X1305	X1306	X1307	X1308	X1309	X1310	X1311	X1312	X1313	X1314	X1315	X1316	X1317	X1318	X1319	X1320	X1321	X1322	X1323	X1324	X1325	X1326	X1327	X1328	X1329	X1330	X1331	X1332	X1333	X1334	X1335	X1336	X1337	X1338	X1339	X1340	X1341	X1342	X1343	X1344	X1345	X1346	X1347	X1348	X1349	X1350	X1351	X1352	X1353	X1354	X1355	X1356	X1357	X1358	X1359	X1360	X1361	X1362	X1363	X1364	X1365	X1366	X1367	X1368	X1369	X1370	X1371	X1372	X1373	X1374	X1375	X1376	X1377	X1378	X1379	X1380	X1381	X1382	X1383	X1384	X1385	X1386	X1387	X1388	X1389	X1390	X1391	X1392	X1393	X1394	X1395	X1396	X1397	X1398	X1399	X1400	X1401	X1402	X1403	X1404	X1405	X1406	X1407	X1408	X1409	X1410	X1411	X1412	X1413	X1414	X1415	X1416	X1417	X1418	X1419	X1420	X1421	X1422	X1423	X1424	X1425	X1426	X1427	X1428	X1429	X1430	X1431	X1432	X1433	X1434	X1435	X1436	X1437	X1438	X1439	X1440	X1441	X1442	X1443	X1444	X1445	X1446	X1447	X1448	X1449	X1450	X1451	X1452	X1453	X1454	X1455	X1456	X1457	X1458	X1459	X1460	X1461	X1462	X1463	X1464	X1465	X1466	X1467	X1468	X1469	X1470	X1471	X1472	X1473	X1474	X1475	X1476	X1477	X1478	X1479	X1480	X1481	X1482	X1483	X1484	X1485	X1486	X1487	X1488	X1489	X1490	X1491	X
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\* NOTICES \*

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a motion compensation arithmetic circuit, and relates to the motion compensation arithmetic unit which performs the motion compensation under dynamic-image coding processing with all heuristics especially.

[0002]

[Description of the Prior Art] In the conventional motion compensation arithmetic circuit, the pixel block of 4 pixel x 4 line is explained as an example.

[0003] (1) Explain the pixel block set as the object of a motion compensation motion compensation. Drawing 13 is drawing showing the searched pixel block set as the object of a motion compensation operation, and a template.

[0004] first, the difference of the pixel to which it corresponds within a pixel block by the formula which is between the searched blocks in the seek area decided on in the template 1 and the front frame 2, and is shown below -- L1 norm which is the absolute value sum, or difference -- either of L2 norms which are the sum of squares is calculated.

[0005]

L1 norm =  $\sum |X_j(i) - Y(i)|$  (i) is a pixel under searched block j started from the front frame 2. (i) - Y (i) | i = 0-15 (1) L2 norm =  $\sum (X_j(i) - Y(i))^2$  i = 0-15 (2) Here, j expresses the number two or more searched blocks were numbered, and is Xj. In drawing 13, the pixel blocks 3-6 are shown as a searched block. It is only that 1 pixel of pixel blocks of j=4-7 is shifted horizontally, and most pixels are common. Moreover, Y (i) is a pixel in a template 1.

[0006] Next, the above (1) Formula Or (2) The number j and the minimum value of the searched block with which L1 norm calculated by the formula or L2 norm serves as min are calculated. The above is the operation performed by the motion compensation.

[0007] About the technique about the above-mentioned motion compensation, for example M. Yamashina, T.Enomoto, T.Kunio, I.Tmaitani, H.harasaki, Y.Endo, T.Nishitani, M.Sato, KKikuchi, and "A Microprogrammable, Real-Time Video Signal Processor (VSP) for Motion compensation", IEEE J.Solid-State Circuits, vol.SC-23, pp.907-915, and Aug.1988. It is indicated.

[0008] Since the difference between the L1 above-mentioned norm and L2 norm is [ which takes an absolute value / or or ] whether to carry out multiplication after calculating a 2-pixel difference, below, it explains only the case where L1 norm is used.

[0009] (2) In all the lap heuristics of the pixel during a searched block, start level or the pixel block which shifted 1 pixel at a time perpendicularly out of a seek area, and consider as a searched block group. Therefore, there is a lap in the pixel during a searched block.

[0010] Drawing 14 is drawing showing the lap during a searched pixel block.

[0011] The front frame 7 consists of 16 pixel x 16 line, and searches the range of \*\*3 pixels from a template 8. In this case, a seek area 9 becomes 10 pixel x 10 line, and the total of the searched block in a seek area 9 is 49. It shifts at a time horizontally 1 pixel of searched blocks 10-13 shown in drawing 14, and pixels X27, X43, X59, and X75 are contained common to these 4 blocks. Moreover, the searched blocks 10, 14-16 of one line have shifted at a time perpendicularly, and pixels X72, X73, X74, and X75 are contained common to these 4 blocks. Especially the pixel X75 is contained common to a total of 16 searched blocks. Therefore, if 1 pixel is read from the memory in which the pixel of the front frame 8 is written, the pixel is applicable to a maximum of 4x4 count

of L1 norm.

[0012] (3) Lap drawing 15 of the pixel between seek areas shows the lap of the seek area to the adjoining template. X21-X26-X170 - X165 The surrounded pixel group is contained common to the seek area 20 to a template 17, and the seek area 9 to a template 8. Furthermore, X85-X90-X170-X165 The surrounded pixel group is contained common to seek areas 20, 9, 21, and 22. Therefore, if 1 pixel is read from the memory in which the pixel of the front frame 7 is written if it doubles with 4x4 times obtained from the lap of the pixel during the above-mentioned searched block, the pixel is applicable to a maximum of 4x4x4 count of L1 norm.

[0013] The example of a Prior art is explained below.

[0014] (4) Prior-art-1 drawing 16 shows drawing for explaining the equipment of the 1st example of the conventional technique which calculates a motion compensation with all heuristics.

[0015] In this drawing, the pixel in a front frame is put on the memory 23 with 2 output ports (P0, P1). The case where 24 to 27 searched block 1 norm which is shown in drawing 16 and which shifted 1 pixel at a time horizontally is calculated is considered. The pixel in a template is put on the memory 30 with 1 output port (P2). 28 are an arithmetic circuit which calculates LPE1 norm. A selector 29 chooses the pixel within the searched block 2427 from the pixel read from the output ports P0 and P1 of memory 23 in the sequence shown in this drawing, and sends it to PE0-PE3, respectively.

[0016] Drawing 17 shows the configuration of PE28 of the 1st example of the conventional technique. The input Bin of PE0 is connected to 30 memory P2. After being latched to the register 33 of PE0, the pixel in the template read from memory 30 shifts between PE one after another, and is transmitted. If it does in this way, within each PE, the sequence of reading the pixel in a template and the pixel within a searched block is in agreement, and L1 norm can be calculated.

[0017] PE0 explains an example in case the searched block 25 and PE2 calculate the searched block 26 and PE3 calculates [ the searched block 24 and PE1 ] the searched block 27.

[0018] Drawing 18 shows the flow of the pixel in the 1st example of a Prior art. The pixel surrounded by the dotted line is a pixel read from the output port P0 among this drawing an output port P1 and except it. Moreover, all over this drawing, the searched block set as the object of L1 norm count is represented with the number of the pixel used as Xj (0 0), and it is shown as L20 and L21 grade that each PE28 is calculating the L1 norm. L1 calculated norm is sent to the minimum value detector 31 from an output C.

[0019] That is, the equipment shown in drawing 16 broadcasts the pixel read from memory 23 using the 1-dimensional lap of the pixel during the searched block which shifted 1 pixel at a time horizontally to PE28, and calculates L1 norm by 4 juxtaposition.

[0020] About the technique about the 1st example of above conventional equipment, it is KM. Yang, M.T. Sun, L. Wu, "Family of VLSI Designs for the motion Compensation Block-Matching Algorithm", IEEE Trans. Circuits and Systems, vol. CAS-36, No. 10, pp 1317-1325, and Oct. 1989, for example. It is indicated.

[0021] (5) Explain the 2nd example of the conventional technique which calculates Prior-art-2 motion compensation with all heuristics.

[0022] Drawing 19 shows drawing for explaining the equipment of the 2nd example of the conventional technique which calculates a motion compensation with all heuristics. The equipment of this drawing is the same configuration as the 1st example of the above-mentioned conventional technique except for a point with 4x4=16 piece PE28. PE0-PE3 calculates the searched blocks 24-27 like the 1st example of a Prior art, and further, PE4 considers the case where the searched block 32 and PE8 calculate the searched block 33, and PE12 calculates the searched block 34, and explains the flow of the pixel in the searched block in that case, and a template.

[0023] Drawing 20 shows the flow of the pixel in the 2nd example of a Prior art.

[0024] By this configuration, they are PE0, PE1, PE2, and --. It sets to -- and PE15 and they are L20, L21, L22, and -- one by one. When -- and count of L71 are completed, they are PE0, PE1, and -- in succession. It sets to -- and PE11 and they are L84, L85, and --. -- and count of L119 can be started. Then, it is read from memory 30, the pass which feeds back the pixel in the template 17 which has shifted between PE to PE0 from PE15 is prepared, and it makes it unnecessary to read the pixel in a template 17 again. However, in order to calculate all L1 norm in the seek area 20 shown in drawing 15, it is required in the scan of a searched block group (it describes as a left scan below) which starts in the count of L20 shown in drawing 20, starts not only in the scan (it is described as a right scan below) of a searched block group finished with count of L119 but in count of the left-hand side of L16, and is finished with count of L115. However, since count of L115 is performed by PE11,

when moving from a left scan to a right scan, as shown in drawing 20, the feedback to P0 from PE15 of the pixel in a template 17 breaks off. Therefore, re-read-out is needed from the memory 30 of a being [ no template 17 ] pixel.

[0025] That is, the equipment shown in drawing 19 broadcasts to PE the pixel which it read 1 pixel at a time perpendicularly from memory 28 horizontally using the two-dimensional lap of the pixel during the searched block which shifted one line at a time, and calculates L1 norm by 4x4 juxtaposition.

[0026] The technique about the 2nd example of equipment is indicated by Tashiro, south, Kasai, and Kaneko" quantity juxtaposition motion compensation computing-element" (Japanese Patent Application No. 4122274) conventionally [ above-mentioned ], for example.

[0027] (6) Explain the 3rd example of the Prior art which calculates conventional technical-3 motion compensation with all heuristics.

[0028] Drawing 21 shows drawing for explaining the equipment of the 3rd example of the conventional technique which calculates a motion compensation with all heuristics.

[0029] The equipment shown in this drawing is the configuration of having transposed the memory 30 holding a template to the memory 39 with 2 output ports (P3, P4), and having added further 4x4 PE28 and one minimum value detector 31, in the equipment of the 2nd example of the above-mentioned conventional technique.

[0030] Drawing 22 shows the flow of the pixel in the 3rd example of the conventional technique. As the term of the lap of the pixel between the seek areas of above (3) showed, there is a lap in the seek area to the adjoining template. Therefore, as shown in drawing 22, two L1 norms are calculable to juxtaposition to the same searched block.

[0031] That is, the equipment shown in drawing 21 can calculate L1 norm by 4x4x2 juxtaposition, though read-out from the memory 23 of a searched block group is the same as that of the 2nd example of the conventional technique.

[0032] They are KM.Yang, M.T.Yang, M.T.Sun, L.Wu, "A Family of VLSI Designs for the Motion Compensation Block-Matching Algorithm", IEEE Trans.Circuits and Systems, vol.CAS-36, nO.10, pp 1317-1325, Oct, and 1989. as well as [ technique / about the 3rd example of the above-mentioned conventional technique ] the 1st example of the above-mentioned conventional technique. It is indicated.

[0033]

[Problem(s) to be Solved by the Invention] However, since PE28 used in the 1st of the above-mentioned conventional technique - the 3rd example had an accumulator in the interior, before structure starts count of L1 complicated and new norm, it has the problem that a register 37 needs to be initialized holding a accumulation value. Moreover, since it is the configuration of 31 transmitting Lminimum value detector 1 norm after calculating L1 norm within each PE28, there is a problem that the pass from all PE28 to the minimum value detector 31 is required.

[0034] Furthermore, the problem that turbulence arises is in feedback of the pixel in the template which has shifted between PE28 since the shift is not made completely when the searched block count is not the integral multiple of 4x4, as explained in the 1st of the conventional technique - the 3rd example.

[0035] Although the above is a problem generated from the structure of PE, 2 pixels per scan of a searched block are further read from the memory holding the pixel of a front frame, and there is a problem generated from distribution of the pixel of broadcasting to all the computing elements of L1 norm calculating. That is, two output ports are required for the memory 23 holding the pixel of a front frame, and since the pass which broadcasts the pixel of a seek area to front PE28 is not vacant until 28 end count of Llast PE1 norm, it has the problem that an invalid cycle arises after count termination of PE0 until it starts count again.

[0036] This invention was made in view of the above-mentioned point, and its pass from all PE to a minimum value detector is unnecessary. The feed back pass of the pixel in a template is unnecessary. Furthermore, again An invalid cycle until it resumes count does not arise after count termination of PE0, but the structure of the computing element which calculates L1 norm is simplified, and it aims at offering the motion compensation arithmetic unit which performs further the motion compensation to which the output port of memory can be managed with one with all heuristics.

[0037]

[Means for Solving the Problem] Drawing 1 shows the principle block diagram of this invention.

[0038] The template 110 whose this invention is the pixel block of m pixel xn line in the present frame, and the horizontal in a seek area Or among all pixel blocks (searched pixel block group) 100 of the m pixel xn line

which shifted 1 pixel at a time perpendicularly the difference of the pixel to which it corresponds within a pixel block -- it is the absolute value sum -- L1 norm In the motion compensation arithmetic unit containing the computing element which calculates L2 norm which is the sum of squares or difference -- The inside of a fields (a right end field is  $m-1$  pixel  $\times b$  line) which divide the seek area of pixel ( $a \times m-1$ )  $\times b$  line in a front frame into the field of  $m$  pixel  $\times b$  line, and are obtained from the memory 121 holding the pixel in a front frame, and memory 121, If it reads 1 pixel at a time and  $m$  pixels is read from the pixel at the left end of Rhine of the top of a left end field At the same time it continues them until it starts and reads  $m-1$  pixel of things for which it reads 1 pixel at a time from the next field It starts moving to the bottom of one line and reading 1 pixel at a time from a left end pixel also in a left end field. In the 1st scan after the 1st scanning termination which reads  $m$  pixels, namely, keeps on reading 2 pixels to coincidence until it finishes reading the  $m \times b$  pixel in a left end field, and  $x(m-1)b$  pixel in the next field The scanning means 122 which repeats a total of  $a-1$  scan until it performs the 2nd scan same as a start point for the pixel at the left end of Rhine of the top of the field which read  $x$  pixel and scans the whole inside of a seek area,  $(m-1)$  The inside of 2 pixels read from memory 121 while the scanning means 122 is performed, A pixel distribution means 120 to have a selection means 124 to choose the pixel of the searched block corresponding to the pixel in the template 110 assigned to each computing element 130, and to send out to a computing element 130, A pixel maintenance means 131 to hold the pixel in the template 110 assigned every computing element 130, the difference of the pixel in the template 110 currently held for the pixel maintenance means 131, and the pixel distributed by the pixel distribution means 120 -- an absolute value or difference -- square -- after calculating a value, the mean value of L1 norm sent from a front computing element or L2 norm is added, and it has the computing element 130 of a  $m \times n$  individual including an operation means 132 to transmit an aggregate value to the following computing element.

[0039] moreover, between the pixels which this invention chose by turns the pixel in the template which adjoined vertically and horizontally including the pixel distribution means, and were distributed by said pixel distribution means -- difference -- an absolute value In the motion compensation arithmetic unit which has a time multiplex means to obtain L1 norm between the template which calculated the value and adjoined these four directions, and a searched block, or L2 norm or difference -- square -- the count which multiplexed the pixel within a searched block -- difference -- an absolute value or difference -- square -- with the 1st register transfer means which chooses the pixel of the searched blocks used for the next count with said pixel selection means, and is sent to the register of the reserve in each computing element, while using it for count of a value difference -- an absolute value and difference -- square -- the timing used for count of a value -- actually -- difference -- an absolute value or difference -- square -- it has the 2nd register transfer means moved to the register used for count of a value.

[0040]

[Function] The pass of this invention from all PE to a minimum value detector is unnecessary, and its feed back pass of the pixel in a template is still more unnecessary, an invalid cycle until it resumes count does not arise after count termination of PE0, but the structure of the computing element which calculates L1 norm is simplified, and the output port of memory can be further managed with one.

[0041]

[Example]

(The 1st example) Drawing 2 shows the configuration of the computing element of the 1st example of this invention. Drawing 3 shows drawing for explaining the equipment of the 1st example of this invention. drawing 2 -- setting -- a computing element SA 41 -- registers 41, 43, 35, and 45 and difference -- the pixel which it consisted of an absolute value computing element 34 and an adder 44, and the pixel inputted from A was inputted into the register 42, and was inputted from B inputs into a register 43 -- having -- difference -- the absolute value computing element 34 -- the difference of a register 42 and a register 43 -- an absolute value is calculated and it outputs to a register 35. next, the difference of a register 35 -- an absolute value and the value inputted from C are added with an adder 44, and the aggregate value is inputted into a register 45. the value -- a register 45 to output port D -- minding -- the following computing element -- or it is outputted to the minimum value detector 31.

[0042] With this configuration, the mean value of accumulation shifts between SAs 41 to the pixel in a template having shifted between PE in PE28 used in the 1st of the conventional technique - the 3rd example. Drawing 4 shows the flow of the pixel in a searched block and a template. The flow of the pixel within a searched block is the same as the 1st of the conventional technique - the 3rd example. On the other hand, although read-out from

memory 30 is the same as that of the 1st of a Prior art - the 3rd example about the pixel in a template, the register 43 in SA0 and Y69= (Y (1)) are latched to the register 43 in SA1, .... Y119 =Y(15) is latched to the register 43 in SA15, and Y68= (Y (0)) is held as it is.

[0043] Only the case where the right scan of the searched block group is carried out is shown in drawing 4 on account of explanation. Although a right scan is performed following a left scan, since there is no pass fed back to PE0 from PE15 in this configuration in fact, the pipeline break when moving from the left scan which became a problem in the 2nd and 3rd example of the conventional technique to a right scan does not arise. Therefore, also when moving from a left scan to a right scan, re-read-out from the memory 30 of the pixel in a template 17 is unnecessary.

[0044] (The 2nd example) Drawing 5 shows the computing element of the 2nd example of this invention. Drawing 6 shows drawing for explaining the arithmetic unit of the 2nd example of this invention.

[0045] This example calculates two L1 norms to the same searched block using there being a lap in the seek area to the adjoining template like the 3rd example of the conventional technique. However, although PE of a twice as many number as this was used in the 3rd example of the conventional technique in order to carry out parallel computing, it calculates by multiplexing in time in this example.

[0046] That is, the registers 51 and 52 which hold the pixel in a template within DSA46, and two registers 53 and 54 which shift the mean value of L1 norm are formed, respectively, and L1 norm to two adjoining templates is calculated by turns.

[0047] Drawing 7 shows the flow of the pixel of the 2nd example of this invention. With this configuration, since the pixel within a searched block will be used for count of 2 times L1 norm, an opening arises for every cycle in a transfer of a pixel. Although there was a problem that an invalid cycle arose, in the 1st of a Prior art - the 3rd example after count termination of PE0 until it started count again since the pass which distributes the pixel of a searched block to all PE28 was not vacant till L1 norm count termination of last PE28, a pixel with the scan of the following seek area-ed can be transmitted with the configuration of this example using this empty cycle.

[0048] The pixel which is vacant in the register 47 in DSA46, and is transmitted to a cycle is latched, and it transmits to a register 48 to the timing which calculates L1 norm by the pixel. L1 norm is calculated using the pixel latched to the register 48, and the pixel in a different template currently held at registers 51 and 52. And L1 calculated norm is sent to the minimum value detector 31 formed corresponding to two templates. In addition, the horizontal arrow head in drawing 7 means transmitting the pixel latched to the register 47 to a register 48. Moreover, it means that the mean value of L1 norm is transmitted and the arrow head of the direction of the diagonal below goes.

[0049] (The 3rd example) Drawing 8 shows the configuration of the computing element of the 3rd example of this invention. Drawing 9 shows drawing for explaining the arithmetic unit of the 3rd example of this invention.

[0050] In this example, four L1 norms are calculated by multiplexing them in time to the same searched block using there being a lap in the seek area to the template which adjoined vertically and horizontally. That is, the registers 56, 57, 58, and 59 which hold the pixel in four different templates within FSA55, and the registers 60, 61, 62, and 63 of four each which shifts the mean value of L1 norm are formed, and L1 norm to four templates which adjoined vertically and horizontally is calculated by turns.

[0051] Drawing 10 shows the flow of the pixel of the 3rd example of this invention. The opening of 3 cycle produces this configuration about a 1-pixel transfer in order to use the pixel within a searched block for count of 4 times L1 norm. Therefore, in this example, it adds to the ability of a pixel with the scan of the following seek area-ed to be transmitted using this empty cycle like the 2nd above-mentioned example. By shifting time amount and transmitting two pixels with the scan of the seek area-ed transmitted to juxtaposition in the 2nd above-mentioned example The selector 29 for choosing a pixel becomes unnecessary, and further, \*\* becomes good as the memory 65 holding the pixel in a front frame also has one output port (P5).

[0052] In addition, the horizontal arrow head in drawing 10 means transmitting the pixel latched to the register 47 to a register 48 like drawing 7 . Moreover, it means that the mean value of L1 norm is transmitted and the arrow head of the direction of the diagonal below goes.

[0053] (The 4th example) Drawing 11 shows the configuration of the computing element FPE 66 of the 4th example of this invention. Drawing 12 shows drawing for explaining the arithmetic unit of the 4th example of this invention.



[0054] The computing element FPE 66 shown in drawing 11 is the same as that of the 3rd above-mentioned example about distribution of the pixel which scanned the seek area and was read from memory 65, and the transfer between registers 47 and 48. On the other hand, after the pixel in a template is inputted into a register 67 from Input Bin and shifts registers 68, 69, and 70, it is transmitted to the following computing element FPE 66. here -- difference -- the difference of the signal with which the selector 49 chose the absolute value computing element 34, and the signal of a register 67 -- an absolute value is computed and it transmits to a register 35. The mean value of L1 norm to four templates which registers 71, 72, 73, and 74 adjoined vertically and horizontally is held, and an adder 44 calculates L1 norm to four templates by turns.

[0055] This example is structure which the pixel in a template shifts between FPE66, and accumulates the mean value of L1 norm within each FRE66 like the 3rd above-mentioned example like [ although four L1 norms are calculated by multiplexing them in time to the same searched block ] PE used in the 1st of the conventional technique - the 3rd example.

[0056] In addition, although only the case where 4x4 parallel operation was performed to the template of 4 pixel x4 line was explained in the above-mentioned example since it was easy, this invention is applicable also to the case where mxn parallel operation is performed, to the template of m pixel xn line.

[0057]

[Effect of the Invention] As mentioned above, according to this invention, the feedback for accumulation becomes unnecessary in the computing element of each of L1 norm calculating. moreover, the pass to a minimum value detector -- final -- the difference of a mxn individual -- it is effective in the structure of the computing element which calculates L1 norm becoming simple that what is necessary is to prepare only in the computing element with which an absolute value is obtained. Furthermore, also when the searched block count calculated when scanning the pixel within a searched block once is not the integral multiple of mxn, the effectiveness that turbulence does not arise is in the pipeline between L1 norm calculating computing elements.

[0058] Furthermore, by calculating L1 norm to the template which adjoined vertically and horizontally by multiplexing it in time, it is vacant on the pass which transmits the pixel in an oxygen-ed field, and a cycle arises. It says [ it ] that count of L1 norm to the next scan can be begun and is effective, without waiting for \*\* to which the last computing element ends count of L1 norm to that scan, after it can transmit a pixel with the scan of the following seek area-ed using this empty cycle and the first computing element ends count of L1 norm to one scan.

[0059] Furthermore, by shifting time amount and transmitting two pixels in the searched block in one scan, \*\* is good as the memory which holds the pixel in a front frame by the pass which distributes a pixel becoming simple also has 1 output port.

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[Translation done.]



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**DESCRIPTION OF DRAWINGS**

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**[Brief Description of the Drawings]**

[Drawing 1] It is the principle block diagram of this invention.

[Drawing 2] It is the block diagram of the computing element of the 1st example of this invention.

[Drawing 3] It is drawing for explaining the arithmetic unit of the 1st example of this invention.

[Drawing 4] It is drawing showing the flow of the pixel of the 1st example of this invention.

[Drawing 5] It is the block diagram of the computing element of the 2nd example of this invention.

[Drawing 6] It is drawing for explaining the arithmetic unit of the 2nd example of this invention.

[Drawing 7] It is drawing showing the flow of the pixel of the 2nd example of this invention.

[Drawing 8] It is the block diagram of the computing element of the 3rd example of this invention.

[Drawing 9] It is drawing for explaining the arithmetic unit of the 3rd example of this invention.

[Drawing 10] It is drawing showing the flow of the pixel of the 3rd example of this invention.

[Drawing 11] It is the block diagram of the computing element of the 4th example of this invention.

[Drawing 12] It is drawing for explaining the arithmetic unit of the 4th example of this invention.

[Drawing 13] It is drawing showing a block and template of the searched pixel set as the object of a motion compensation operation.

[Drawing 14] It is drawing showing the lap during a searched pixel block.

[Drawing 15] It is drawing showing the lap of the seek area to the adjoining template.

[Drawing 16] It is drawing for explaining the equipment of the 1st example of the conventional technique.

[Drawing 17] It is the block diagram of the computing element used in the 1st of the conventional technique - the 3rd example.

[Drawing 18] It is drawing showing the flow of the pixel in the 1st example of the conventional technique.

[Drawing 19] It is drawing for explaining the equipment of the 2nd example of the conventional technique.

[Drawing 20] It is drawing showing the flow of the pixel in the 2nd example of the conventional technique.

[Drawing 21] It is drawing for explaining the equipment of the 3rd example of the conventional technique.

[Drawing 22] It is drawing showing the flow of the pixel in the 3rd example of the conventional technique.

**[Description of Notations]**

1, 8, 17, 18, 19, 40, 64 Template

2 Seven Before frame

3, 4, 5, 6, 10, 11, 12, 13, 14, 15, 16, 24, 25, 26, 27, 32, 33, 34 Searched pixel block

9, 20, 21, 22 Seek area

23 Memory with 2 Output Ports Holding Pixel in Front Frame

28 Computing Element Used in the 1st of the Conventional Technique - 3rd Example

29, 35, 49, 50 Selector

30 Memory with 1 Output Port Holding Template

31 Minimum Value Detector

32, 33, 35, 27, 42, 43, 45, 47, 48, 51, 52, 53

54, 56, 57, 58, 59, 60, 61, 62, 63, 67, 68, 69

70, 71, 72, 73, 74 Register

34 Difference -- Absolute Value Computing Element

36, 44 adders

38 Rye State Buffer

39 Memory with 2 Output Ports Holding Template

41 Computing Element Used in the 1st Example of this Invention  
46 Computing Element Used in the 2nd Example of this Invention  
55 Computing Element Used in the 3rd Example of this Invention  
65 Memory with 1 Output Port Holding Pixel in Front Frame  
66 Computing Element Used in the 4th Example of this Invention  
100 Searched Block  
110 Template  
120 Pixel Selection Means  
121 Memory  
122 1st Scanning Means  
123 2nd Scanning Means  
124 Selection Means  
130 Computing Element  
131 Pixel Maintenance Means  
132 Operation Means

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[Translation done.]

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**CLAIMS**

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[Claim(s)]

[Claim 1] The template which is the pixel block of  $m$  pixel  $xn$  line in the present frame, and the horizontal in a seek area Or among all pixel blocks (searched pixel block group) of the  $m$  pixel  $xn$  line which shifted 1 pixel at a time perpendicularly the difference of the pixel to which it corresponds within a pixel block -- it is the absolute value sum -- L1 norm In the motion compensation arithmetic unit containing the computing element which calculates L2 norm which is the sum of squares or difference -- The inside of a fields (a right end field is  $m-1$  pixel  $xb$  line) which divide the seek area of pixel  $(am-1)$   $xb$  line in a front frame into the field of  $m$  pixel  $xb$  line, and are obtained from the memory holding the pixel in a front frame, and this memory, If it reads 1 pixel at a time and  $m$  pixels is read from the pixel at the left end of Rhine of the top of a left end field At the same time it continues them until it starts and reads  $m-1$  pixel of things for which it reads 1 pixel at a time from the next field It starts moving to the bottom of one line and reading 1 pixel at a time from a left end pixel also in a left end field. Read  $m$  pixels, namely, it sets reading 2 pixels to coincidence on the 1st scan after the 1st scanning termination continuously until it finishes reading the  $mxb$  pixel in a left end field, and  $x(m-1)$   $b$  pixel in the next field. The scanning means which repeats a total of  $a-1$  scan until it performs the 2nd scan same as a start point for the pixel at the left end of Rhine of the top of the field which read  $xb$  pixel and scans the whole inside of a seek area,  $(m-1)$  The inside of 2 pixels read from this memory while this scanning means is performed, A pixel distribution means to have a selection means to choose the pixel within the searched block corresponding to the pixel in the template assigned to this each computing element, and to send out to this computing element, A pixel maintenance means to hold the pixel in this template assigned for this every computing element, the difference of the pixel in this template currently held for this pixel maintenance means, and the pixel distributed by this pixel distribution means -- an absolute value or difference -- square -- the motion compensation arithmetic unit characterized by having the computing element of a  $m \times n$  individual including an operation means to add the mean value of L1 norm sent from a front computing element, or L2 norm, and to transmit an aggregate value to the following computing element after calculating a value.

[Claim 2] between the pixels which chose by turns the pixel in the template which adjoined vertically and horizontally including said pixel distribution means, and were distributed by said pixel distribution means -- difference -- an absolute value In the motion compensation arithmetic unit which has a time multiplex means to obtain L1 norm between the template which calculated the value and adjoined these four directions, and a searched block, or L2 norm or difference -- square -- the count which multiplexed the pixel within a searched block -- difference -- an absolute value or difference -- square -- with the 1st register transfer means which distributes the pixel of the searched blocks used for the next count with said pixel distribution means, and is sent to the register of the reserve in each computing element, while using it for count of a value difference -- an absolute value and difference -- square -- the timing used for count of a value -- actually -- difference -- an absolute value or difference -- square -- the motion compensation arithmetic circuit characterized by having the 2nd register transfer means moved to the register used for count of a value.

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[Translation done.]